Design Example Report

Title	***60W DC-DC Power Supply using DPA426R***
Specification	Input: 36 - 72VDC Output: 12V / 5A
Application	Distributed Power Architectures
Author	Power Integrations Applications Department
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Summary and Features

This report describes a design for Distributed Power Architecture power supply, featuring the following:

- Uses DPA426R
- 36-72 VDC input
- 12V / 60 W output
- Low component count
- Integrated fault protection

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

1 Introduction

This document is an engineering report describing a single output Flyback converter employing the DPA426R - an integrated IC comprising a high voltage MOSFET and a fully featured PWM controller. The input voltage range is 36 to 72VDC providing a regulated +12V at 5A.

This document contains the power supply specification, schematic, and bill of materials, transformer documentation, printed circuit layout, and performance data.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	36	48	72	V_{DC}	
No-load Input Power ($60V_{DC}$)				1	W	
Output						
Output Voltage 1	V_{OUT1}	12.1	12.75	13.4	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}			5	A	
Total Output Power						
Continuous Output Power	P_{OUT}			60	W	
Peak Output Power	P_{OUT_PEAK}			75	W	
Efficiency	η	82			%	Measured at Max. P_{OUT}, 25 ^{o}C
Ambient Temperature	T_{AMB}	0		40	^{o}C	Free convection, Sea level

Table 1 – Power Supply Specification

3 Schematic

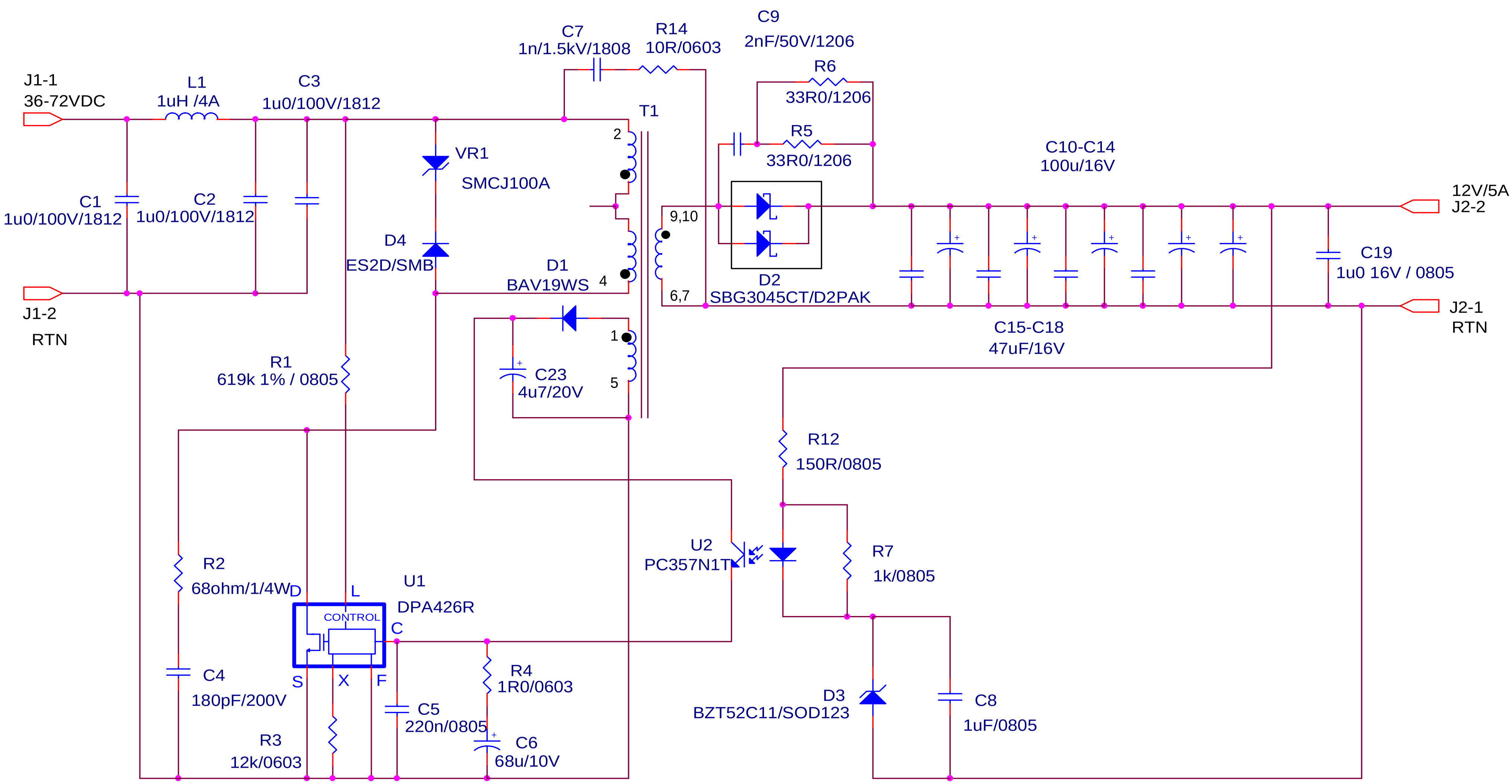

Figure 1 - Schematic

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4 Circuit Description

4.1 Primary Side Circuit

Figure 1 shows a single-ended Flyback converter using the DPA426R. The circuit is designed for 36 V to 72 V input range and provides a single +12V @ 5A output. C1 and L1 provide input filtering. C2 and C3 bypass the DC rail. The DC rail is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. D4 and VR1 clamp the maximum voltage transients at the Drain of U1 caused by energy stored in the leakage inductance of the transformer.

R1 is used to set the low line turn-on threshold to approximately 33 V, and also sets the over-voltage shutdown level to approximately 88 V. C5 bypasses the U1 control pin, and provides the peak current necessary for driving the ***DPA-Switch*** internal MOSFET. C6 has three functions. It provides the energy required by U1 during startup, sets the auto-restart frequency during fault conditions, and also reduces the gain of U1 as a function of frequency. R4 adds a zero to stabilize the power supply control loop. R2 and C4 are snubber components that reduce high frequency oscillations on the Drain-source voltage waveform.

4.2 Output Rectification

The output of T1 is rectified and filtered by D2 and C10-C18. An auxiliary Flyback winding on T1 powers U1 during normal operation. This winding delivers energy during the off time of U1 (e.g. the flyback period), with an output voltage proportional to the supply output voltage. The turns-ratio of T1 sets the output voltage of the auxiliary winding to approximately 12 V. D1 and C23 rectify and filter the auxiliary winding output.

4.3 Output Feedback

Zener Diode (D3) and the opto-coupler (U3) photo-diode voltage drop set the output voltage. R12 and R7 bias the opto-coupler and zener diode. The opto-coupler output also provides power to U1 during normal operating conditions.

5 PCB Layout

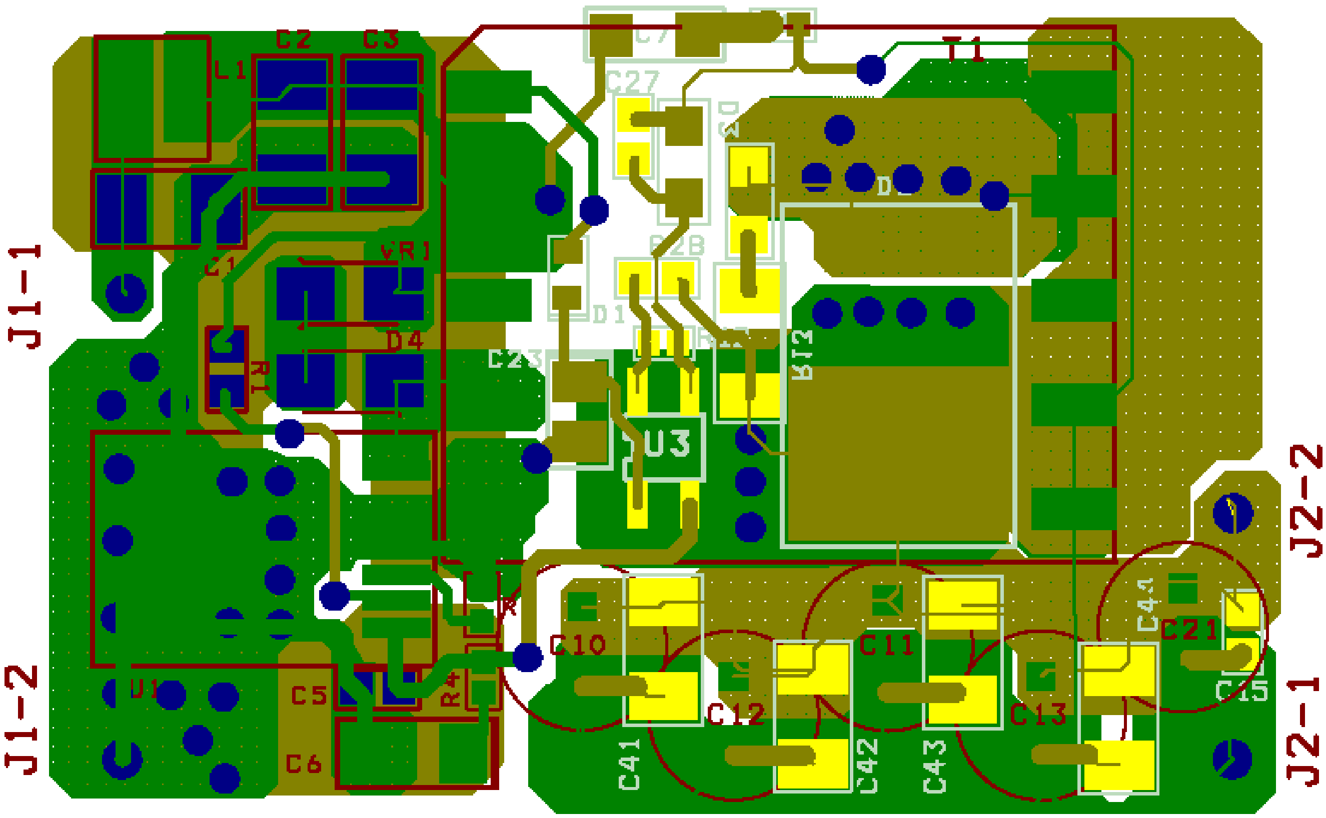

Figure 2 - Printed Circuit Layout.

6 Bill Of Materials

Flyback Converter Bill Of Materials

Item	Qty	Reference	Description	Manufacturer	Part Number
1	3	C1-C3	1u0/100V/1812		
2	1	C4	180pF/200V		
3	1	C5	220n/0805		
4	1	C6	68u/10V		
5	1	C7	1n/1.5kV/1808		
6	2	C8, C19	1uF/0805		
7	1	C9	2.2nF/50V/1206		
8	1	C15	1u0 16V / 0805		
9	1	C23	4u7/20V		
10	5	C10-C14	100u/16V	Sanyo	16SA100M
11	4	C15-C18	47uF/16V	TDK	C5750X5R1C476M
12	1	D1	BAV19WS	Diodes, Inc.	
13	1	D2	SBG3045CT/D2PAK	Diodes, Inc.	
14	1	D3	BZT52C11/SOD123	Diodes, Inc.	
15	1	D4	ES2D/SMB	Diodes, Inc.	
16	1	L1	1uH /4A		
17	1	R1	619k 1% / 0805		
18	1	R2	68ohm/1/4W		
19	1	R3	12k/0603		
20	1	R4	1R0/0603		
21	2	R5, R6	33R0/1206		
22	1	R7	1k/0805		
23	1	R12	150R/0805		
24	1	R14	10R/0603		
25	1	T1	Custom Flyback Transformer		
26	1	U1	DPA426R	Power Integrations	
27	1	U2	PC357N1T	Sharp	
28	1	VR1	SMCJ100A	Diodes, Inc.	

Table 2 - Flyback Converter Bill Of Materials

7 Transformer Specification

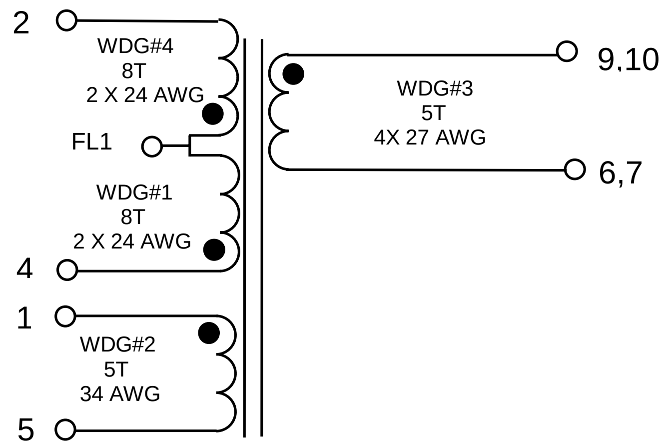

Figure 3 - Transformer Diagram.

7.1 Electrical Specifications

Electrical Strength	1 second, from Pins 1-4 to Pins 5-8	1500 VDC
Creepage	Between Pins 1-4 and Pins 5-8	N/A
Primary Inductance	Pins 1,4, all other windings open, measured at 400KHz, 400mVRMS	21 μH, ±10 %
Resonant Frequency	Pins 1,4, all other windings open	3.0 MHz (Min.)
Primary Leakage Inductance	Pins 1,4, with Pins 5-8 shorted, measured at 400KHz, 400mVRMS	1 μH (Max.)

7.2 Materials

Item	Description
[1]	Core: EFD25-3F3 or equivalent gap for A_L of 84 nH/T^2
[2]	Bobbin: 10 pin surface mount
[3]	Magnet Wire: #27 AWG Double Coated
[4]	Magnet Wire: #34 AWG Double Coated
[5]	Magnet Wire: #24 AWG Double Coated
[6]	Tape, Polyester
[7]	Varnish

Table 3 – Transformer BOM

7.3 Transformer Build Diagram

7.4 Transformer Construction

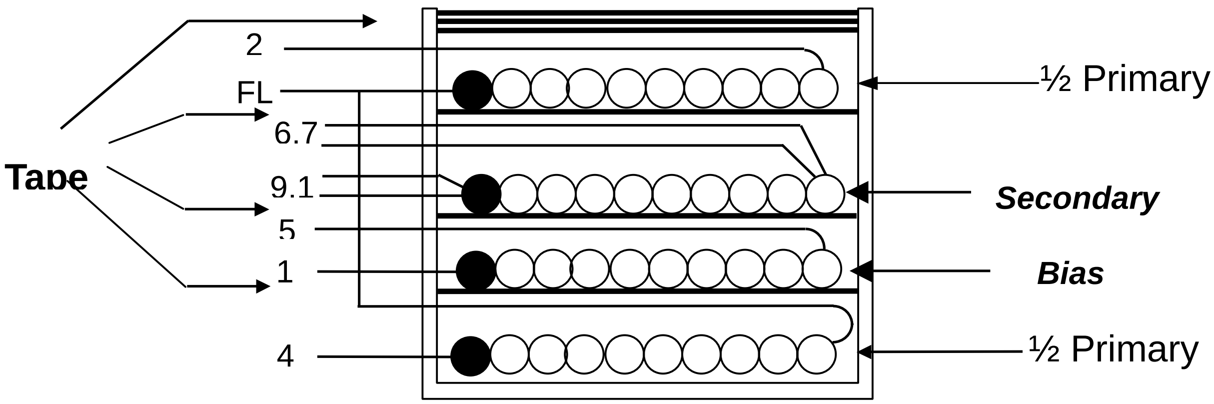

Figure 4– Transformer construction

½ Primary	Start at Pin 4. Wind 8 bifiliar turns of item [5]. Finish on Exit-finish lead at bobbin flange slot on primary side of bobbin, leaving 1" lead length.
Basic Insulation	Use one layer of item [6] for basic insulation.
Bias Winding	Start at Pin 1. Wind 5 turns of item [4] Finish on Pin 5.
Basic Insulation	Use one layer of item [6] for basic insulation.
Secondary Winding	Start at Pins 9 and 10. Wind 5 quadrifiliar turns of item [3] Finish on Pins 6 and 7.
Basic Insulation	Use one layer of item [6] for basic insulation.
½ Primary	Start in bobbin flange slot on primary side of transformer leave 1" lead length at start. Wind 8 bifiliar turns of item [5]. Finish on Pin 2.
Outer Wrap	Wrap windings with 3 layers of tape [item [5].
Flying Lead Finish	Twist start of winding 4 together with finish of winding 2. Tin and trim to 1/8" length (FL1).
Final Assembly	Assemble and secure core halves. Varnish and impregnate (item [7]).

8 Transformer Spreadsheets

A	B	D	F	G	I
DPASwitch_Flyback_Rev_1e_090302; Copyright Power Integrations Inc. 2002	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**DPASwitch_Flyback_090302 - Continuous/Discontinuous mode Spreadsheet. Copyright 2002 Power Integrations**
ENTER APPLICATION VARIABLES					**12V/5A**
VDCMIN	36			Volts	Minimum DC Input Voltage
VDCMAX	72			Volts	Maximum DC Input Voltage
VO	12			Volts	Output Voltage
PO	60			Watts	Output Power
n	0.83				Efficiency Estimate
Z			0.7		Loss Allocation Factor, (0.7 Recommended)
VB	12			Volts	Bias Voltage
UV AND OV PARAMETERS					
		min	max		
VUVOFF		29.3	32.4	Volts	Minimum undervoltage On-Off threshold
VUVON		31.5	33.9	Volts	Maximum undervoltage Off-On threshold (turn-on)
VOVON		73.1	-	Volts	Minimum overvoltage Off-On threshold
VOVOFF			92.4	Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			603.1	k-Ohms	Line Sense Resistor
ENTER DPASWITCH VARIABLES					
DPASWITCH	**dpa426**			*16VDC*	*36VDC*
Chosen Device	*DPA426*		*Power Out*	*43W*	*100W*
ILIMITMAX	*6.5*	*7.5*		Amps	From DPASWITCH Data Sheet
Frequency	*f*				Enter 'F' for fS = 400KHz and 'L' for fS = 300KHz
fS	400000			Hertz	DPASWITCH Switching Frequency
VOR	**41**	***Warning***	**41**	Volts	Reflected Output Voltage not recommended above 40V. Reduce VOR
KI	1.00		1		Current Limit Reduction Factor
ILIMITEXT			6.500	Amps	Minimum External Current limit
RX			-	k-Ohms	Resistor from X pin to source to set external current limit
VDS	2.5			Volts	DPASWITCH on-state Drain to Source Voltage
VD	0.5			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KRP/KDP	**0.50**				Ripple to Peak Current Ratio (0.2 < KRP < 1.0 : 1.0< KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**efd25**				
Core Manuf					
Bobbin Manuf					
Core		*EFD25*		*P/N:*	*EFD25-3F3-Exxx-xx*
Bobbin		*EFD25_Bobbin*		*P/N:*	*52.2*
AE			0.58	cm^2	Core Effective Cross Sectional Area
LE			5.7	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			16.4	mm	Bobbin Physical Winding Width
M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	**2**				Number of Primary Layers
NS	**5**				Number of Secondary Turns

Transformer spreadsheet continued…

CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.55		Maximum Duty Cycle
IAVG			2.01	Amps	Average Primary Current
IP			4.86	Amps	Peak Primary Current
IR			2.43	Amps	Primary Ripple Current
IRMS			2.76	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			19	uHenries	Primary Inductance
NP			16		Primary Winding Number of Turns
NB			5		Bias Winding Number of Turns
ALG			72	nH/T^2	Gapped Core Effective Inductance
BP			1320	Gauss	Peak Flux density during transients (Limit to 4000 Gauss)
BM		***Warning***	988	Gauss	Peak Flux density<2000 Gauss, A smaller core may be used
BAC			247	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1564		Relative Permeability of Ungapped Core
LG			**0.98**	mm	Gap Length (Lg >> 0.051 mm)
BWE			32.8	mm	Effective Bobbin Width
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			15.96	Amps	Peak Secondary Current
ISRMS			8.17	Amps	Secondary RMS Current
IO			5.00	Amps	Power Supply Output Current
IRIPPLE			6.46	Amps	Output Capacitor RMS Ripple Current
VOLTAGE STRESS PARAMETERS					
VDRAIN			178	Volts	Maximum Drain Voltage (Includes Effect of Leakage Inductance)
PIVS			34	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			34	Volts	Bias Rectifier Maximum Peak Inverse Voltage
ADDITIONAL OUTPUTS					
V_OUT2				Volts	Auxiliary Output Voltage
VD_OUT2				Volts	Auxiliary Diode Forward Voltage Drop
N_OUT2			0.00		Auxiliary Number of Turns

Table 4 – Transformer Spreadsheet

9 Performance Data

All measurements performed at room temperature.

9.1 Efficiency

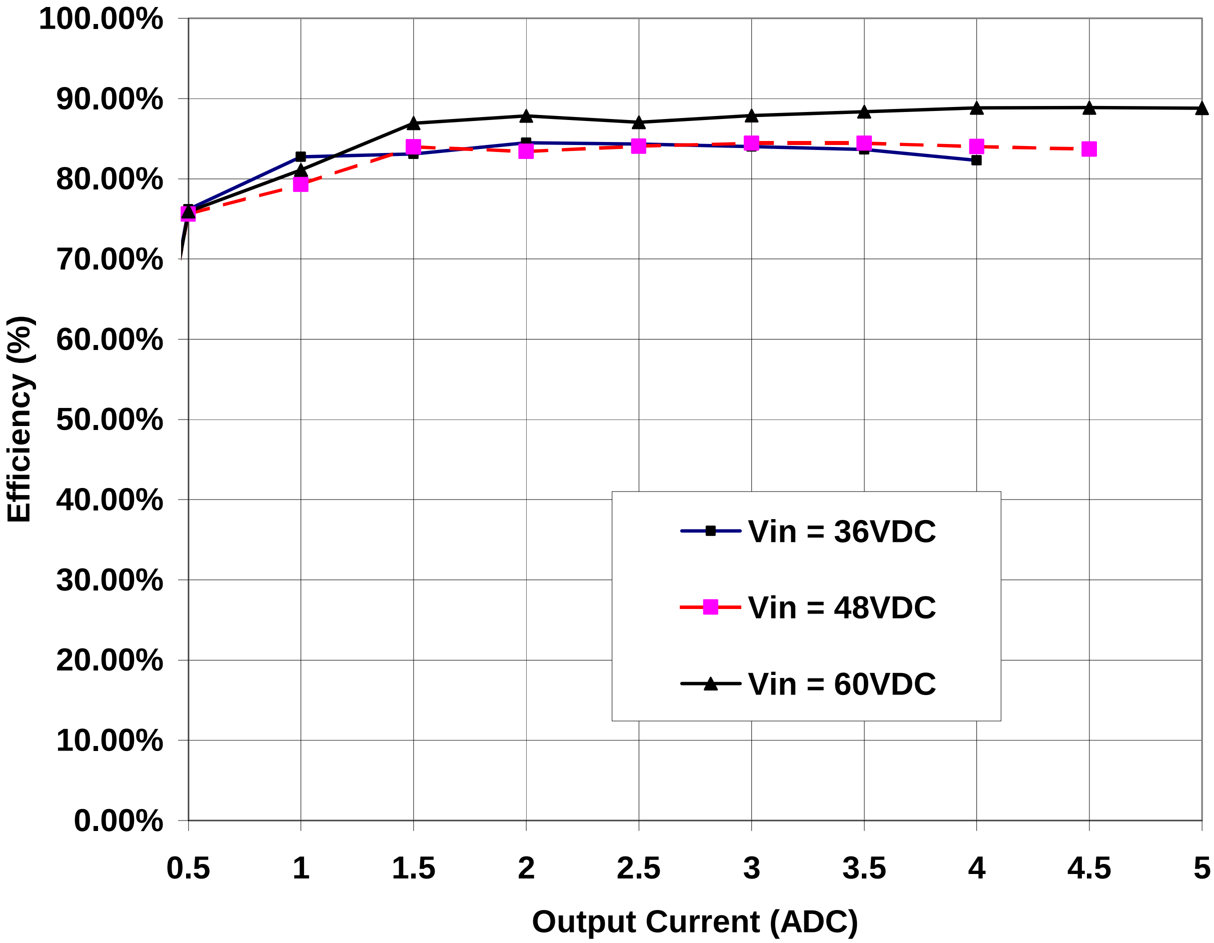

Figure 5 - Efficiency vs. Load Current, Room Temperature

9.2 Regulation

9.2.1 Load

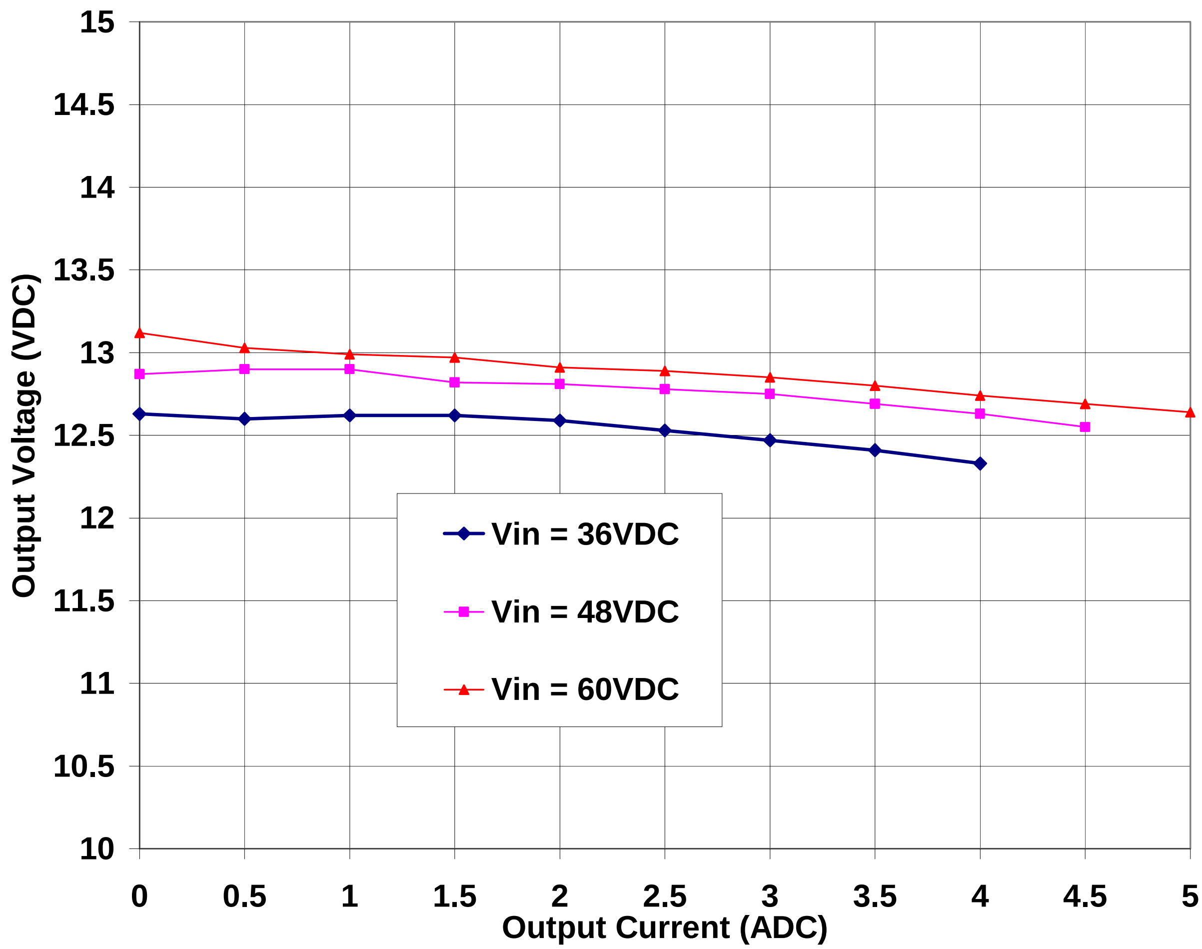

Figure 6- Load Regulation, Room Temperature

9.2.2 Line

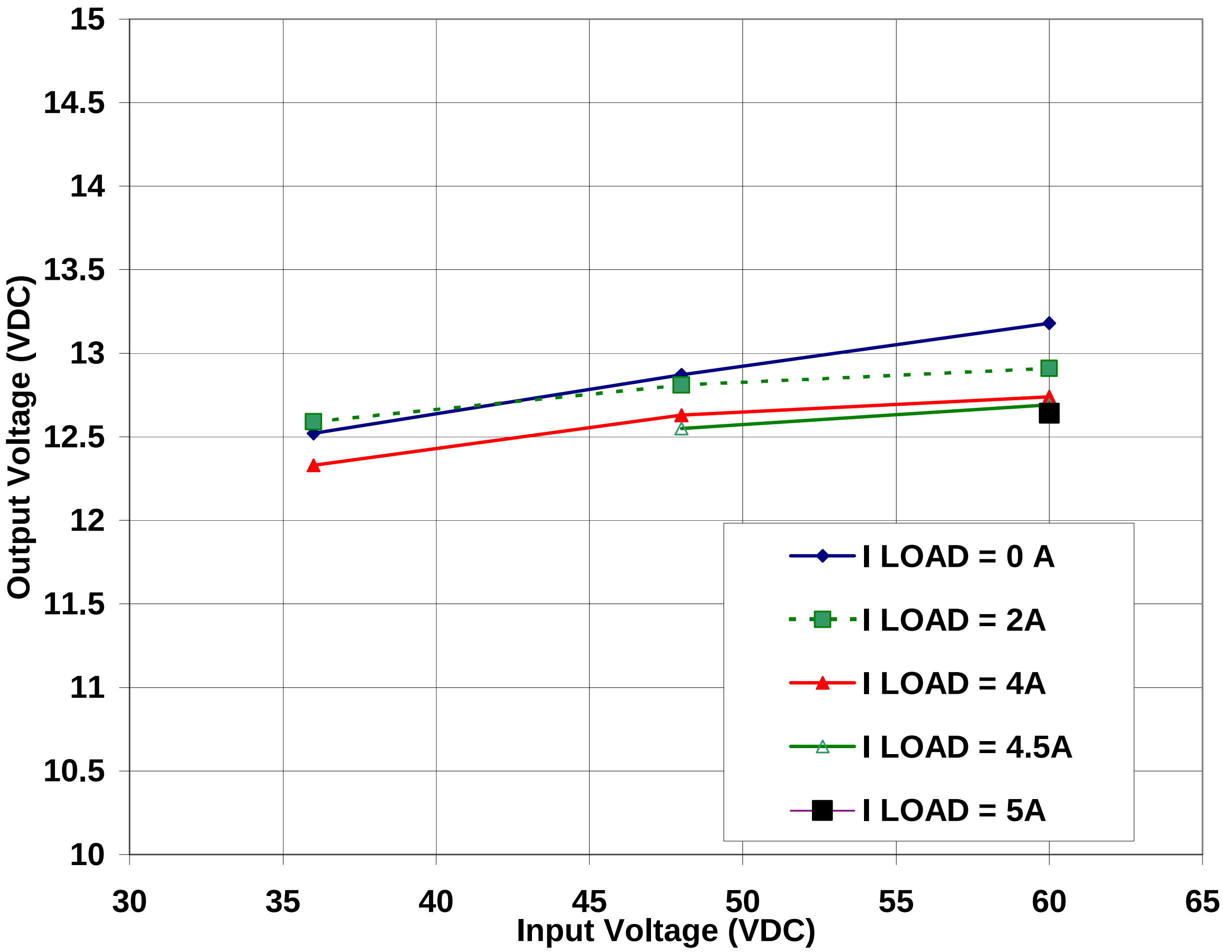

Figure 7 - Line Regulation, Room Temperature

10 Waveforms

10.1 Drain Voltage, Normal Operation

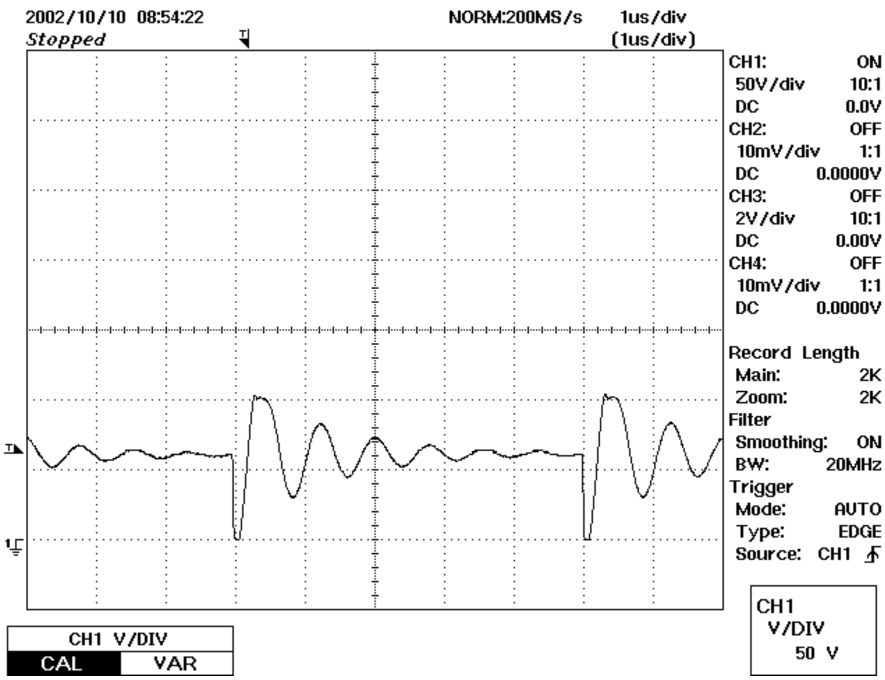

Figure 8 - 60VDC No Load- VDS, 20V / div

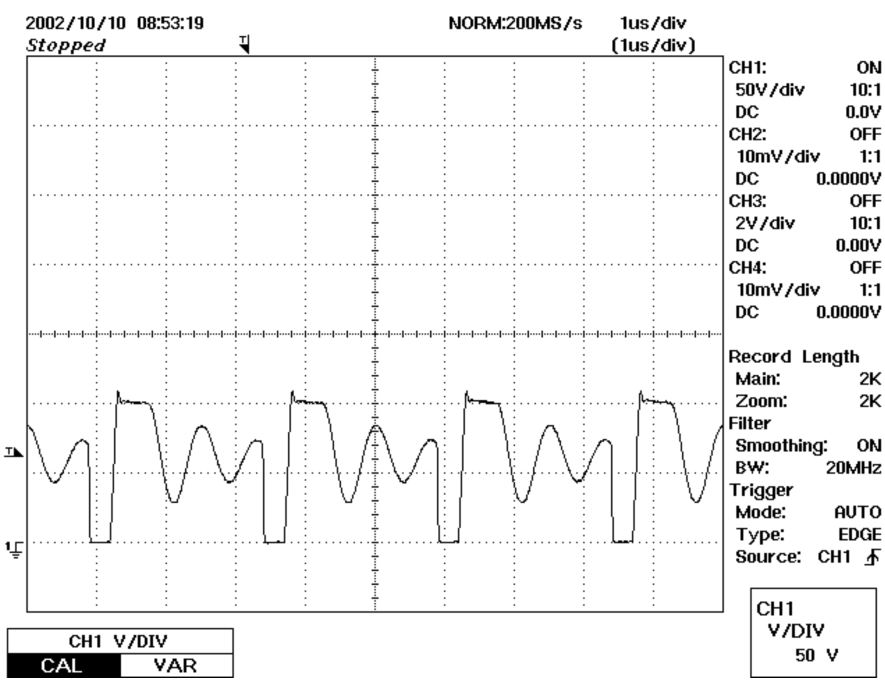

Figure 9 – 60VDC I = 5A - VDS 20V / div

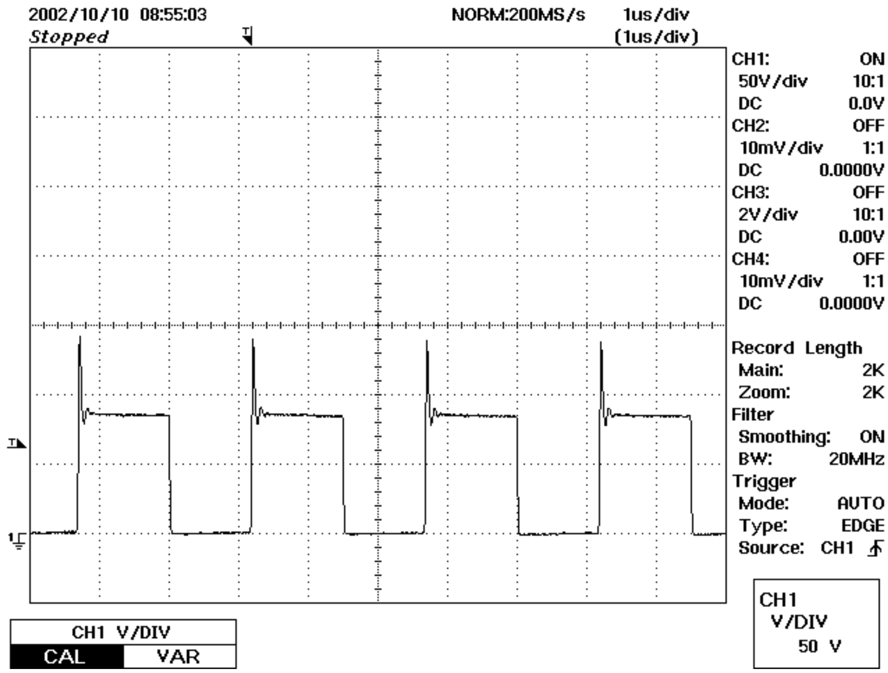

Figure 10 - 48VDC I = 2.5A - VDS, 50V / div

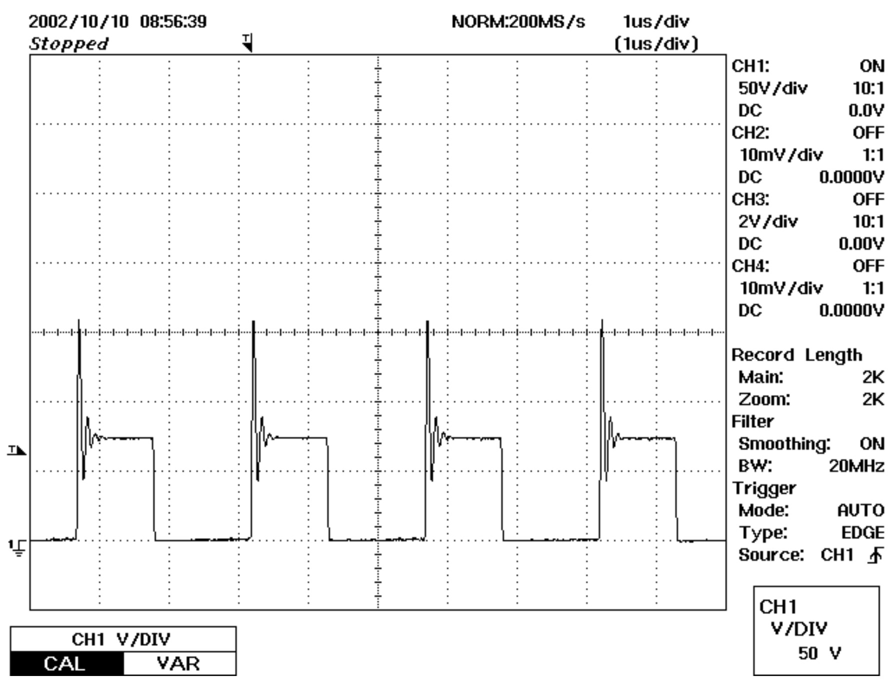

Figure 11 - 36VDC I = 4A - VDS, 50V / div

10.2 Output Voltage Start-up Profile

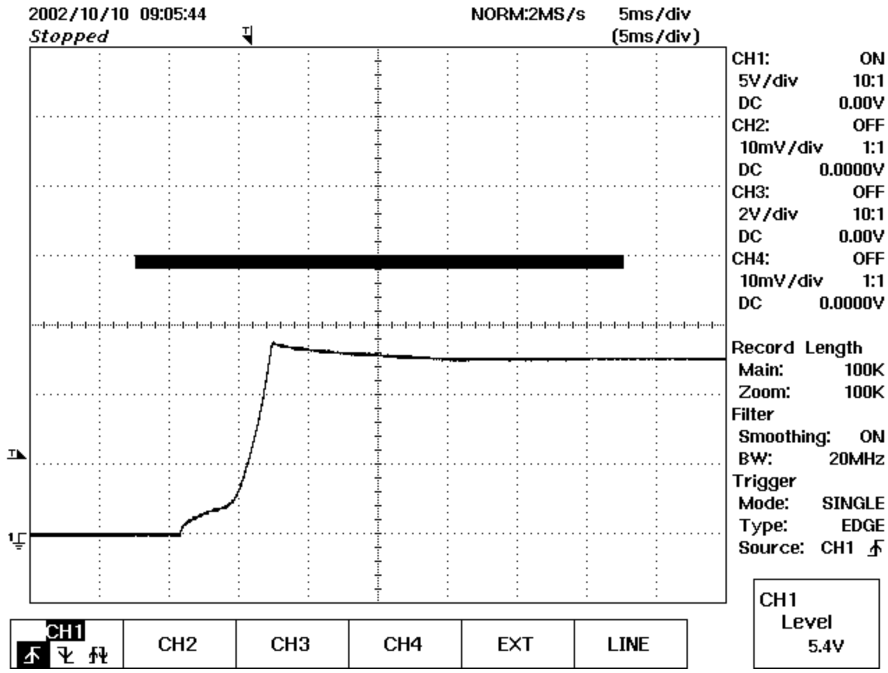

Figure 12 - Start-up Profile, Vin = 48V, No Load (5msec/div) & (5V/div)

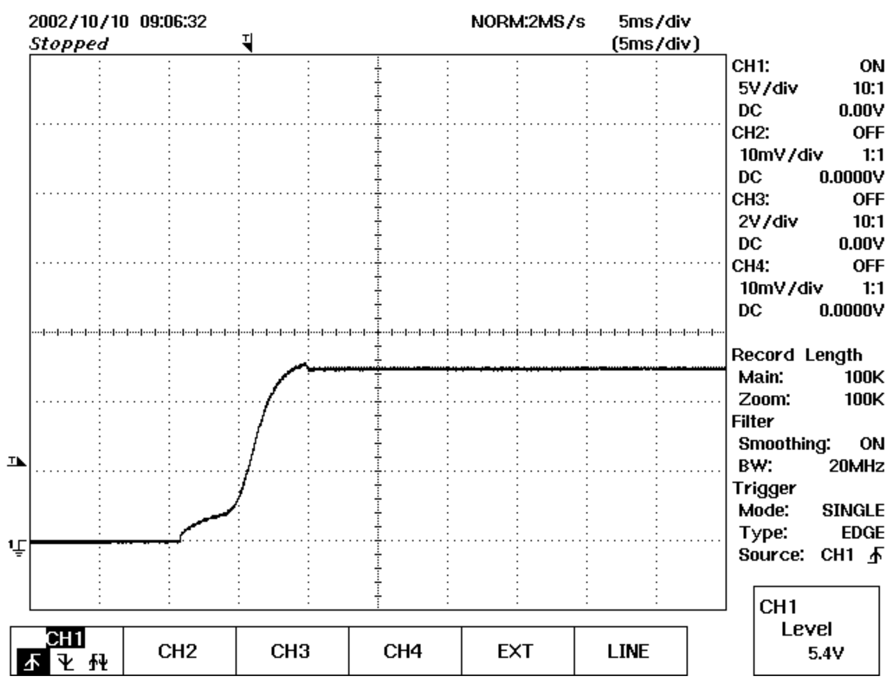

Figure 13 - Start-up Profile, Vin = 48V, I = 4.5A (5msec/div) & (1V/div)

10.3 Output Ripple Measurements

10.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 14 and Figure 15.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

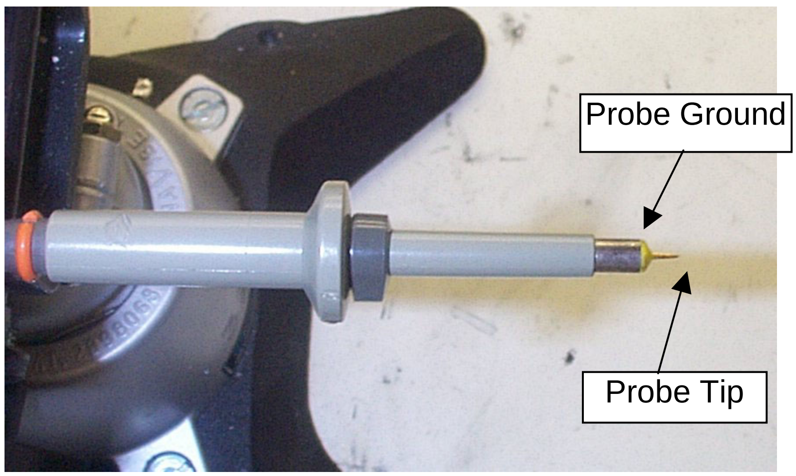

Figure 14 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

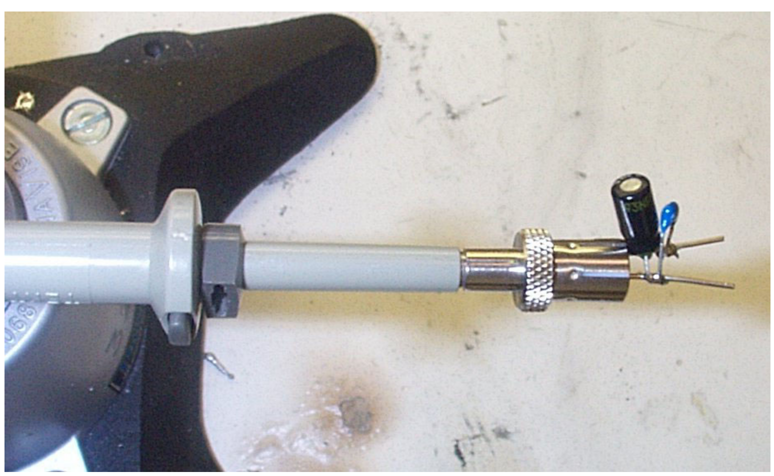

Figure 15 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

10.3.2 Measurement Results

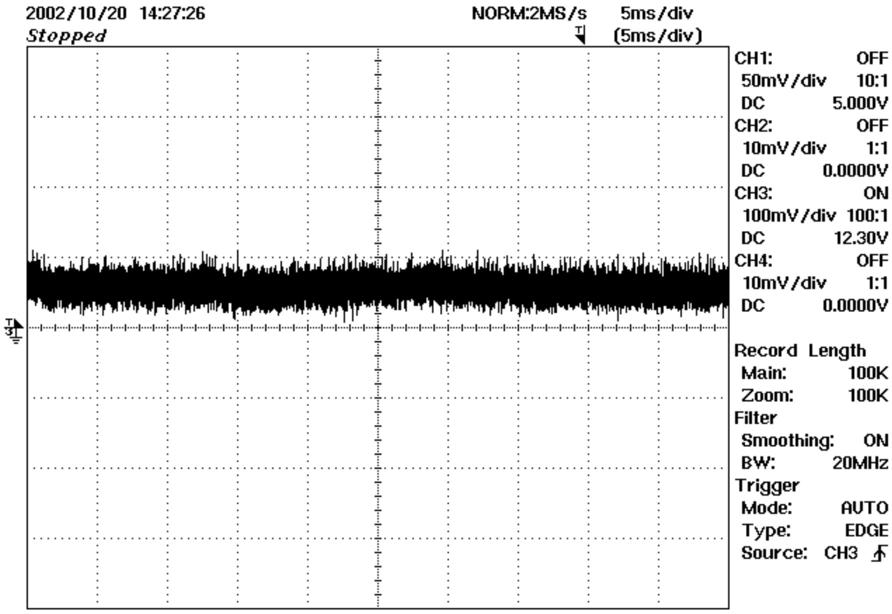

Figure 16 - Vin = 36VDC, I = 4A (5 ms, 50 mV / div)

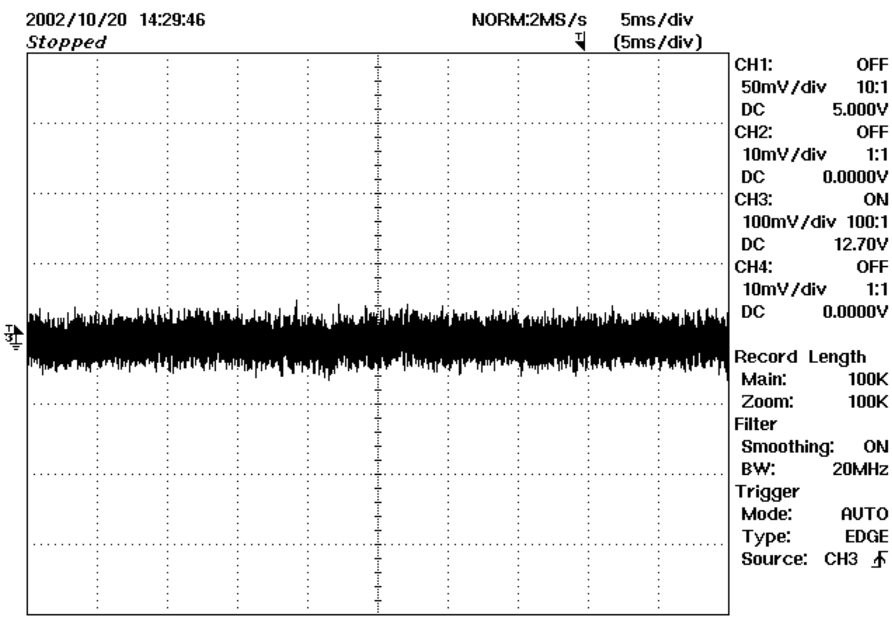

Figure 17 - Vin = 60VDC, I = 5A (5 ms, 50 mV / div)

11 Revision History

Date	Author	Revision	Description & changes	Reviewed
March 30, 2004	RSP	1.0	Initial release	VC / AM

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