Design Example Report

Title	*100 W Output Automotive Power Supply for 400 V Systems Using InnoSwitch™ 3-AQ INN3990CQ*
Specification	150 V_{DC} – 400 V_{DC} Input; 13.5 V / 7.35 A Output
Application	12 V Auxiliary Battery Replacement
Author	Automotive Systems Engineering Department
Document Number	DER-953Q
Date	August 14, 2023
Revision	1.0

Summary and Features

- Ultra-compact design for 400 V_{DC} BEV automotive applications
- Low component count (only 66 components)[1] design with a single 900 V power switch
- Full load operation from 150 V_{DC} to 500 V_{DC} input[2]
- Reinforced 500 V isolated transformer (IEC-60664-1 and IEC-60664-4 compliant)
- ≥92% full load efficiency across the input voltage range
- 1% output voltage load and line regulation
- Secondary-side regulated output
- Ambient operating temperature from -40 °C to 85 °C
- Complete fault protection, including output current limit and short-circuit protection
- Uses automotive-qualified AEC-Q surface mounted (SMD) components[3]
- Low profile, 22 mm height

[1] Power conversion stage only, excluding input and output ports. See Figure 5
[2] Derated power below 150 V_{DC} input. See Figure 93
[3] AEC-Q200 transformer qualification and AEC-Q qualified SR MOSFET selection belong to final design.

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Disclaimer:

1 Introduction

This engineering report describes a 100 W single-output automotive power supply intended for 400 V battery system electric vehicles. The design supports a wide input range of 150 V_{DC} to 500 V_{DC}. This design uses the 900 V rated INN3990CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (output) sides by observing the creepage and clearance requirements according to IEC-60664 parts 1 and 4.

The report contains the power supply specification, schematic diagram, printed circuit board (PCB) layout, bill of materials (BOM), magnetics specifications, and performance data.

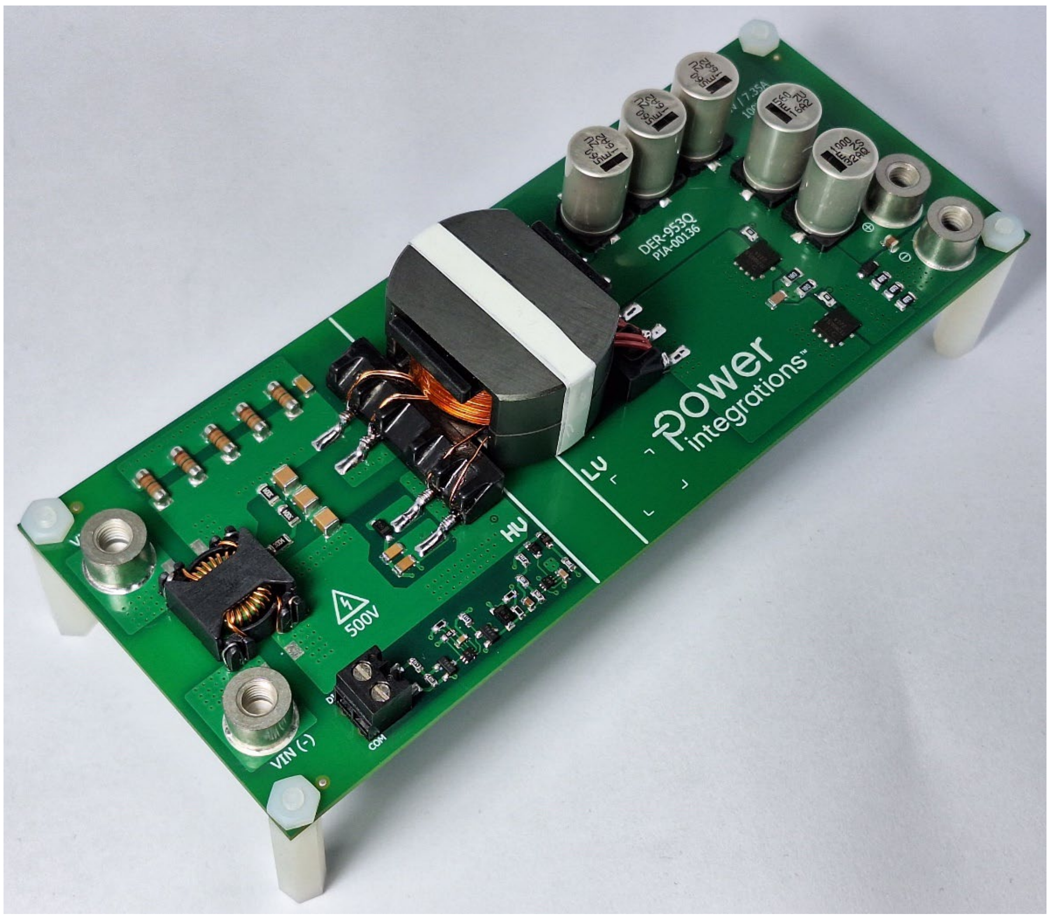


Figure 1 – Populated Circuit Board, Entire Assembly.

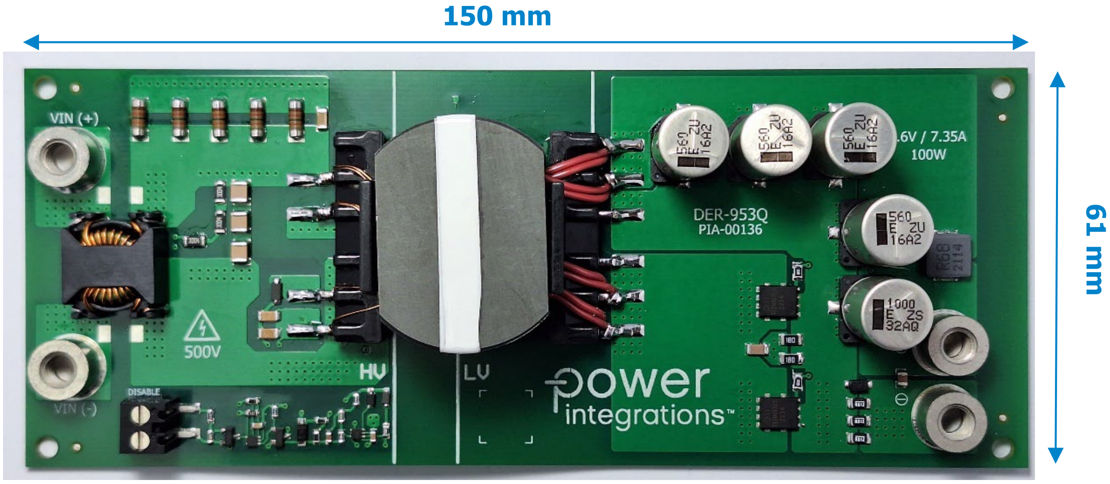


Figure 2 – Populated Circuit Board, Top.

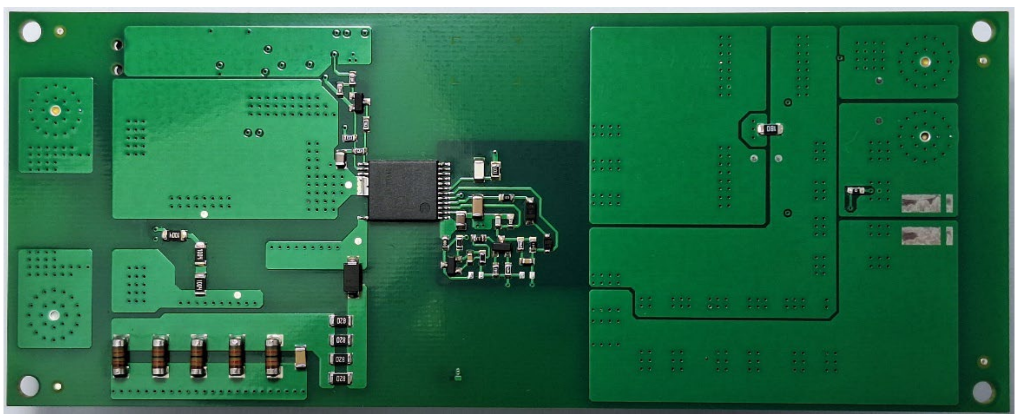


Figure 3 – Populated Circuit Board, Bottom.

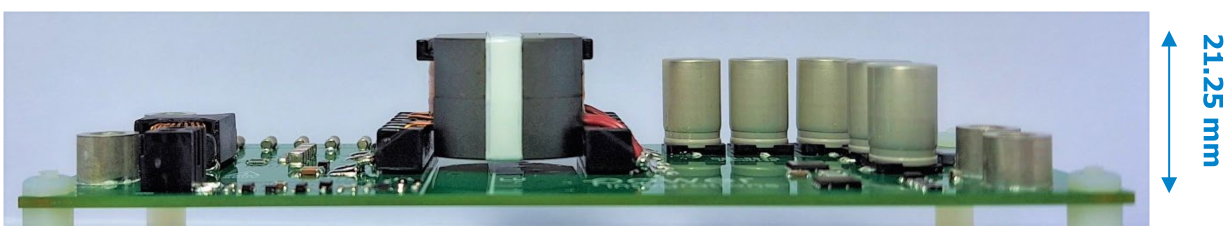


Figure 4 – Populated Circuit Board, Side.

The design can deliver continuous 100 W output power at 85 °C ambient temperature from 150 V_{DC} to 500 V_{DC} input voltage range. The 13.5 V output configuration allows the design to replace a vehicle's auxiliary battery, helping reduce weight and lessen maintenance.

The InnoSwitch3-AQ IC maintains necessary regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary side via FluxLink™. Secondary-side controls synchronous rectification for improving the overall efficiency compared to diode rectification, thus saving cost and space by eliminating the need for a heat sink.

2 Design Specification

The following tables below represent the performance of the design.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV**	150[4]	380	500	V_{DC}
Operating Switching Frequency	f_{SW}	25		43	kHz
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	V_{OUT}	13.3	13.5	13.7	V_{DC}
Ripple Voltage Measured on Board	V_{RIPPLE}			270	mV
Output Current Parameters					
Output Current	I_{OUT}		7350		mA
Output Power Parameters					
Continuous Output Power at 150 V_{DC} – 500 V_{DC} Input	P_{OUT}		100[5]		W
Output Overshoot and Undershoot During Dynamic Load Condition	ΔV_{OUT}	-450		450	mV

Table 1 – Electrical Specifications.

[4] Lower input voltage is possible but with output power derating.
[5] For maximum output power capability at V_{IN} less than 150 V, see Section 12.

2.2 Isolation Coordination

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3990CQ	**BV_{DSS}**			900	V
System Voltage	**V_{SYSTEM}**			750	V
Working Voltage	**$V_{WORKING}$**			500	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175			
Rated Impulse Voltage	**$V_{IMPULSE}$**			2.5	kV
Altitude Correction Factor for h_a	**c_{ha}**	1.59			
Basic Clearance Distance Requirement	**CLR_{BASIC}**	2.4			mm
Reinforced Clearance Distance Requirement	**$CLR_{REINFORCED}$**	4.8			mm
Basic Creepage Distance Requirement for PCB	**$CPG_{BASIC(PCB)}$**	3.2			mm
Reinforced Creepage Distance Requirement for PCB	**$CPG_{REINFORCED(PCB)}$**	6.4			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	**V_{ISO}**	3534			V_{RMS}
Partial Discharge Test Voltage	**V_{PD_TEST}**	1080			V_{PK}

Table 2 – Isolation Coordination[6].

2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		85	°C
Altitude of Operation	ha			5500	m

Table 3 – Environmental Specifications.

[6] Clearance and creepage distances are derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

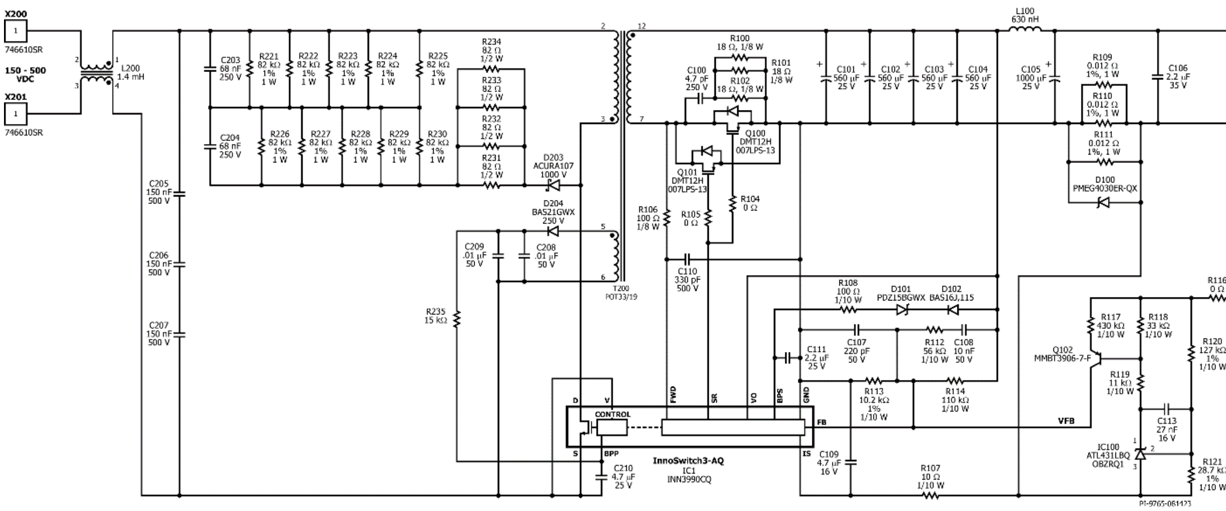


Figure 5 – DER-953Q Power Conversion Stage.

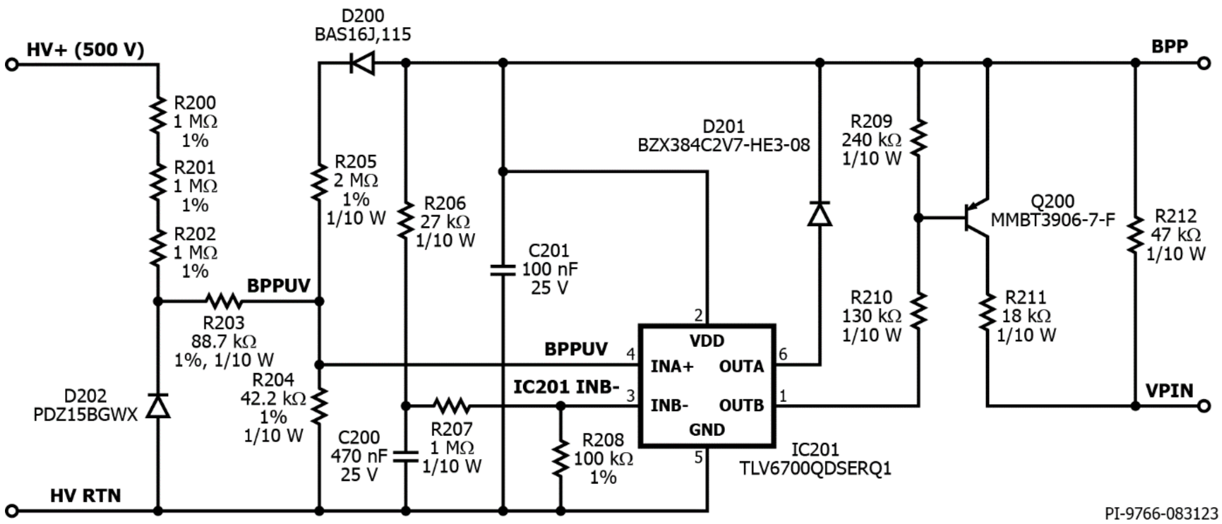


Figure 6 – DER-953Q Start-up Circuit and InnoSwitch3-AQ Enable/Disable

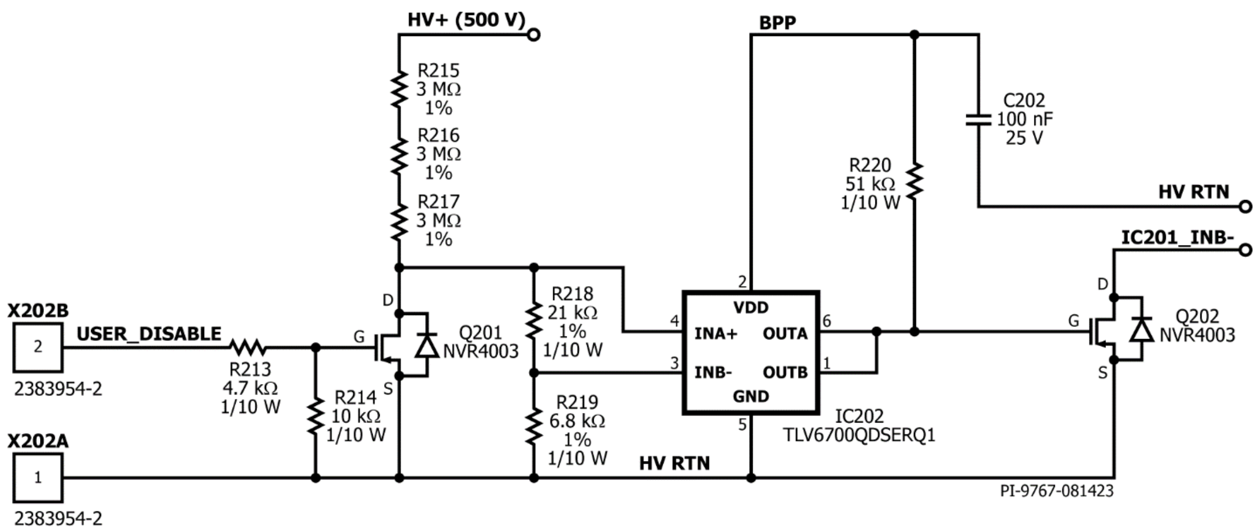


Figure 7 – DER-953Q UV/OV Circuit and User Disable.

4 Circuit Description

4.1 Input Filter

Common mode choke L200 and bypass capacitors C205 to C207 help filter input noise. C205 to C207 are also used to minimize the primary side current loop. The capacitors are selected not to exceed 65% of their voltage rating and to maintain enough pad-to-pad distance to meet creepage and clearance requirements.

4.2 High-Voltage Side Circuit

The circuit design uses a flyback converter topology to provide an isolated low-voltage output from the high-voltage input. The flyback transformer T200 primary winding is connected across the high-voltage DC input and the drain terminal of the 900 V GaN power MOSFET switch internal to INN3990CQ (IC200).

An R2CD-type snubber circuit is placed across the primary side winding to limit the drain-source voltage peaks seen by the internal GaN MOSFET switch during turn-off. A super-fast (or better) surface mount, AEC-Q qualified diode should be used. Diode D203 meets creepage and clearance requirements and ensures that the reverse voltage across the diode would not exceed 70-75% rating. Capacitors C203 and C204 catch the energy from the leakage inductance of transformer T200. The capacitor values are selected to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation throughout the switching period. Resistors R221 to R230 dissipate the energy stored by the snubber capacitors. The resistor values are selected such that their average voltage will not exceed 80% of their voltage rating and dissipate less than 50% of their rated power.

IC200 is self-starting, using an internal high-voltage current source to charge the BPP capacitor (C210).

The transformer T200 auxiliary winding provides power to the primary side of IC200 during normal operation. This minimizes the power derived from the internal high-voltage current source, improving overall efficiency, and reducing heating of IC200. The auxiliary winding output is rectified and filtered by diode D204 and capacitors C208 and C209. Current is fed to the BPP pin through resistor R235.

4.3 Low-Voltage Side Circuit

The secondary side of the INN3990CQ (IC200) provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR FETs Q100 and Q101 rectify the voltage across the secondary winding of the transformer T200, which is then filtered by output capacitors C102 to C104. An RC-type snubber formed by resistors R100 to R102 and capacitor C100 dampens the high-frequency ringing in the SR FET drain-source nodes.

The secondary-side controller inside IC200 controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed from the FWD pin via resistor

R106. Capacitor C110 and resistor R106 form a low pass filter that reduces the voltage spike seen by the FWD pin during SR turn-off and ensures that the maximum rating of 150 V will not be exceeded.

In continuous conduction mode, the primary-side power MOSFET is turned off before the secondary-side controller requests a new switching cycle to the primary. In discontinuous conduction mode, the SR FET is turned off when the voltage across it falls below $V_{SR(TH)}$[7]. Secondary-side control of the primary-side power MOSFET removes the possibility of cross-conduction of the two switches and ensures reliable synchronous rectifier operation.

The secondary-side of IC200 is powered by either the secondary winding forward voltage (thru R106 and the FWD pin) or the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C111 via an internal regulator.

Diodes D101, D102, and resistor R108 serve as a secondary-side output overvoltage protection (secondary OVP). During output overvoltage events, current will be injected to the BPS pin of IC200 through these components and triggers the IC to operate in auto-restart (AR) mode.

The INN3990CQ has an FB pin internal reference of 1.265 V. Resistors R113 and R114 form the basic voltage divider feedback network for InnoSwitch3-AQ designs. For this design, the output voltage value set by R113 and R114 is 10-15% higher than the rated output voltage as a requirement for implementing the *Precise Voltage Regulation* circuit. Capacitor C107 provides decoupling from high-frequency noise affecting power supply operation. Capacitor C108 and resistor R112 form a feedforward network to speed up the feedback response time and lower the output ripple.

Output current is sensed by monitoring the voltage drop across parallel resistors R109 to R111. The resulting current measurement is filtered using R106 and C109 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of around 35 mV is used to reduce losses. Once the threshold is met, IC200 will control the number of pulses to maintain a fixed output current. The IC enters auto-restart (AR) operation when the output voltage falls below 90% of regulation and recovers when the load current is reduced below the CC limit. Diode D100 limits the voltage drop across R109 to R111 to protect the IS pin during overload or short circuit conditions.

4.4 Precision Voltage Regulation (PVR) Circuit [8]

The PVR circuit improves output voltage regulation by using an external error amplifier with a high-precision reference voltage (ATL431) to control the FB pin. The PVR injects a DC bias current to the FB pin of IC200 to reduce the DC error at the output. The ATL431 error amplifier network is placed after the output filter inductor L100 and current sense resistors R109 to R111 to compensate for voltage drops.

The ATL431LIBQDBZRQ1 is selected for its high precision and stability across temperatures. The output voltage is sensed through voltage dividers R120 and R121. The

[7] Refer to InnoSwitch3-AQ datasheet for $V_{sr(TH)}$

[8] Circuit implementation is optional. Application is only necessary if output voltage regulation needs to be within 1%.

resistor values are chosen such that at the rated output voltage, the voltage across the REF pin of IC100 equals the reference voltage of 2.5 V. IC100 sinks cathode current proportional to the difference between the scaled output voltage and its internal reference. The amount of cathode current affects the amount of current injected into the FB node. Capacitor C113 lowers the bandwidth of the PVR circuit so that it only corrects for DC error.

Resistors R118 and R119 provide the base current path for Q102 and bias current to IC100. Together with R117, the values of these resistors are chosen such that IC100 and Q102 are kept away from saturation and provide an adequate allowance for the base and cathode currents to swing during load transients. While operating in the forward active region, it can be interpreted that Q102 acts as a variable impedance in parallel to the upper feedback resistor R114.

4.5 BPP Pull Down Circuit [9]

In some situations, the DC-Link capacitors are not fully discharged during shutdown and manifest as residual voltage in the DC link. This residual voltage can appear as a non-monotonic input to the INN3990CQ, leading to an indeterminate state during power-up. This happens when the input voltage is below 20 V, which causes the internal current source to be incapable of stably charging the BPP capacitor. The pull-down circuit clips the BPP voltage below 3.1 V when the input voltage is below 20 V. IC200 BPP pin is pulled down when the input voltage is within 20 V to 23 V and released when the input voltage is within 26 V to 29 V. The 3 V between 23 V to 26 V is the recommended hysteresis between BPP pull-down and BPP release.

Comparator IC201 TLV6700QDSERQ1 is a low quiescent current window comparator with an internal temperature-stable 400 mV reference. Resistors R200 to R204 works as a voltage divider connected to the INA+ pin of IC201 to sense the input voltage. Diode D200 and R205 are the hysteresis components used to inject additional current to R204 after IC200 BPP is released. Comparator IC201 OUTA is pulled low if the voltage at IC201 INA+ is less than 400 mV.

4.6 InnoSwitch3 Enable-Disable

The V pin of the IC200 INN3990CQ can be used to implement a remote enable/disable function.

The IC200 INN3990CQ is enabled when the current injected into the V pin is between the UV/OV pin brown-in threshold (I_{UV+} = 30.4 μA) and the UV/OV pin line overvoltage threshold (I_{OV+} = 98 μA). It is turned off otherwise.

Resistor R212 injects the enable current ($I_{UV+} < I_{VPIN} < I_{OV+}$). Resistors R209 to R211 and Q200 are used to inject additional current to disable IC200 ($I_{VPIN} > I_{OV+}$). Transistor Q200 is ON when IC201 OUTB is low.

[9] Circuit implementation is optional. Application is only necessary when low line input voltage stability cannot be guaranteed.

4.7 InnoSwitch3 Temporary Enable [10]

When the V pin is used for enable-disable, a circuit is needed to ensure that IC200 is enabled temporarily. The recommended temporary enable period is 10 ms to 30 ms. This is only required during the initial power-up, giving enough time for IC200 to process information and avoid overheating when disabled from start-up.

Resistor R206 and C200 are used for time delay and are computed to have a 10 ms time constant. 3 time constants should be enough to reach 95% of steady-state voltage. R207 and R208 is a voltage divider tuned to ensure that the voltage at IC201 INB- goes above the 400 mV reference within the recommended temporary enable period. Comparator IC201 OUTB is pulled low if the voltage at IC201 INB- is greater than 400 mV, disabling IC200.

4.8 Alternative Input Overvoltage/Undervoltage circuit [11]

An alternative circuit is needed to implement line overvoltage and undervoltage detection when IC200 VPIN is used for the enable-disable function. IC202 TLV6700DSERQ1 window comparator is used for detecting line OV/UV. Resistor R215 to R219 are voltage dividers to set the undervoltage and overvoltage triggers. Resistor R220 is used to pull up the open drain output of IC200.

Enable from undervoltage is triggered when $V_{R218} + V_{R219} > 400$ mV; IC202 OUTA becomes open, resulting in Q202 turning ON, pulling down IC201 INB-. Disable due to overvoltage is triggered when $V_{R219} > 400$ mV; IC202 OUTB is pulled low, resulting in Q202 turning OFF, releasing IC201 INB-. Enable from undervoltage is set at 130 V. Disable at overvoltage is set at 530 V.

Users can design alternative input monitoring circuits as long as the logic going to the Q202 gate is consistent with what is described in this section.

4.9 User Enable and Disable

Users can disable the power supply unit (PSU) by applying 5 V at ports X202B-X202A. This will trigger Q201 ON, pulling down IC202 INA+.

[10] Circuit implementation is optional. Application is only necessary to avoid heating when VPIN is used for enable-disable. New chip versions have a fix on the heating.
[11] Circuit implementation is optional. Application is only necessary when OV/UV is needed but VPIN is used for enable-disable.

5 PCB Layout

Layers:	Six (6)
Board Material:	FR4
Board Thickness:	1.6 mm
Copper Weight:	1 oz

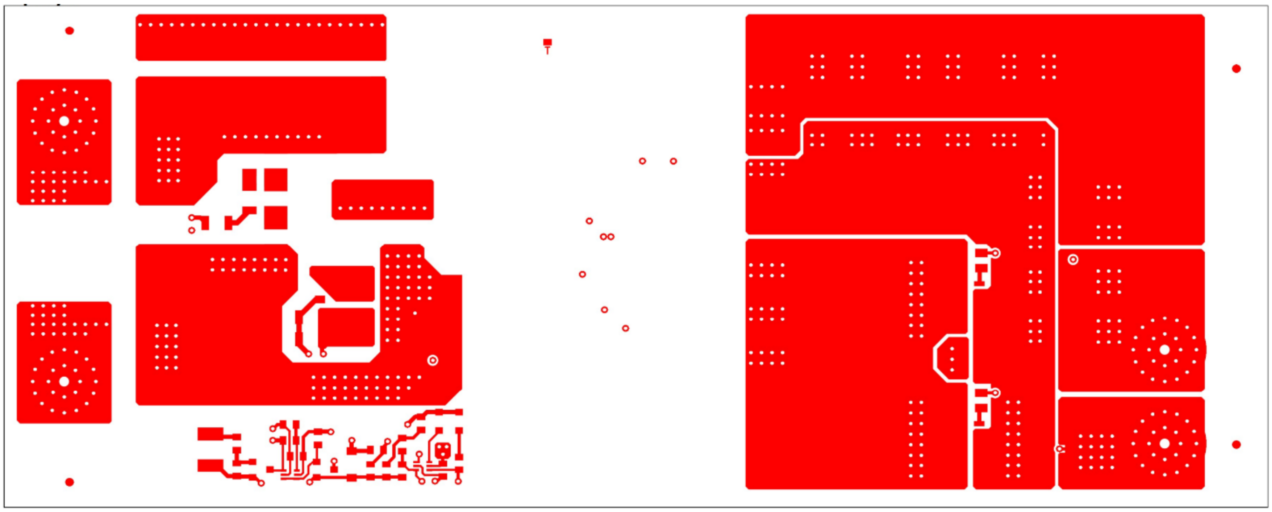


Figure 8 – DER-953Q Top Layer PCB Layout.

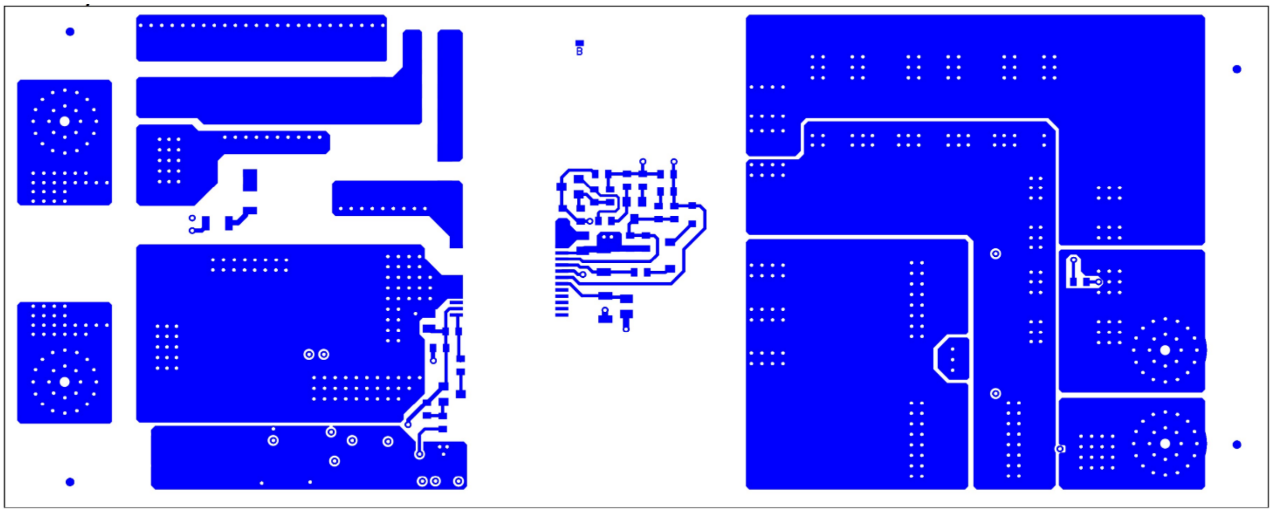


Figure 9 – DER-953Q Bottom Layer PCB Layout.

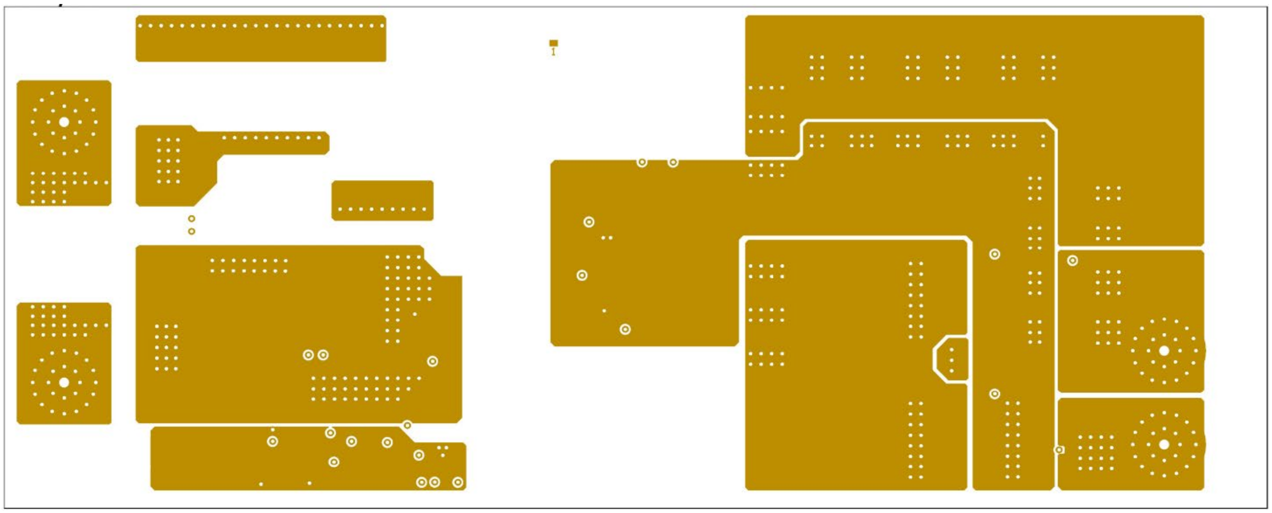


Figure 10 – DER-953Q Mid-Layer 1 PCB Layout.

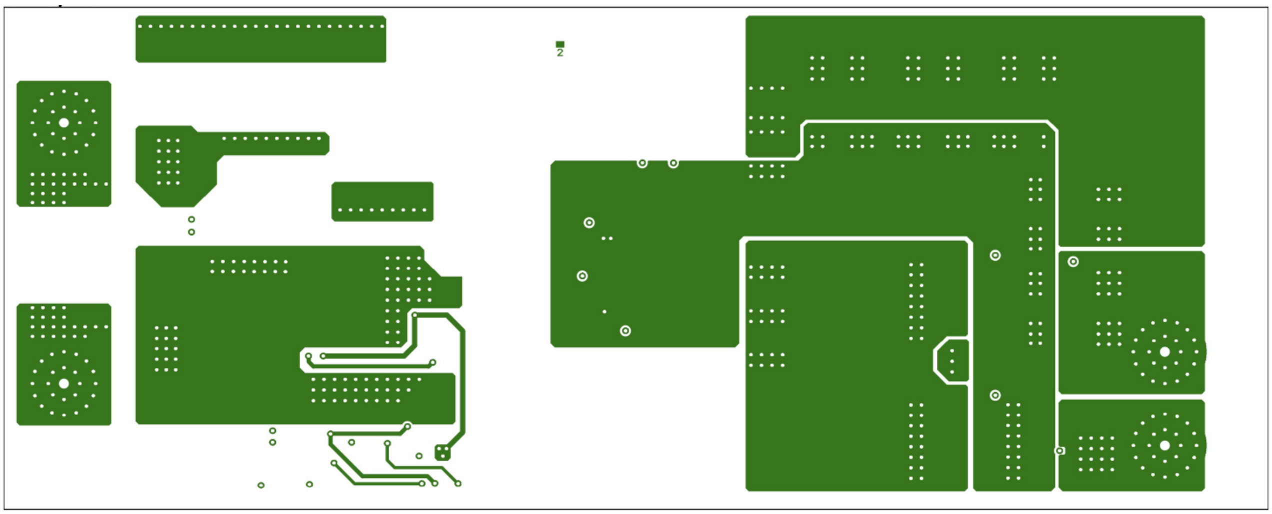


Figure 11 – DER-953Q Mid-Layer 2 PCB Layout.

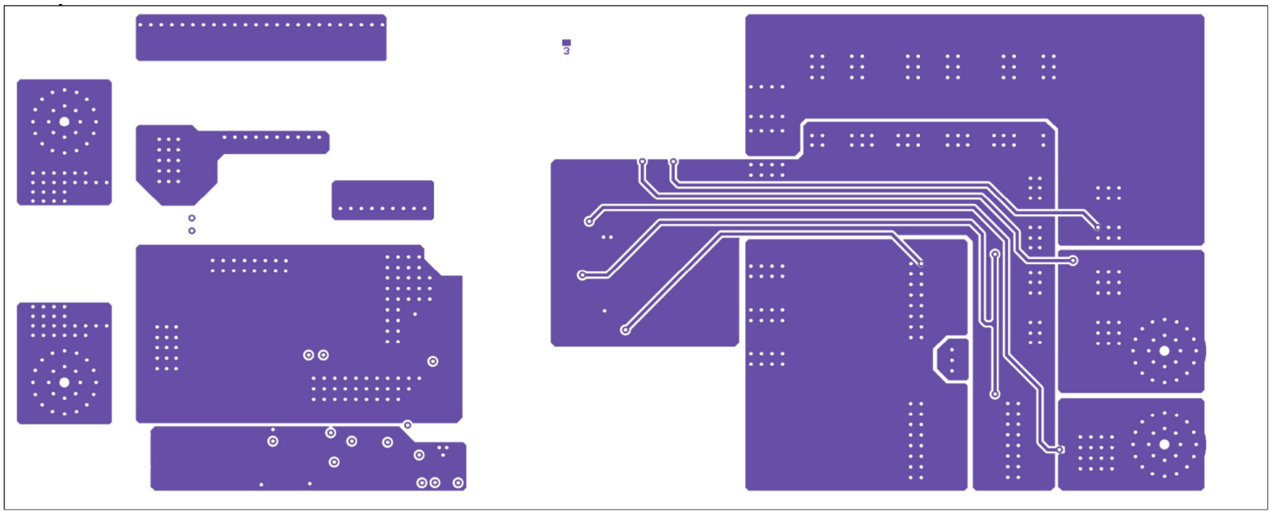


Figure 12 – DER-953Q Mid-Layer 3 PCB Layout.

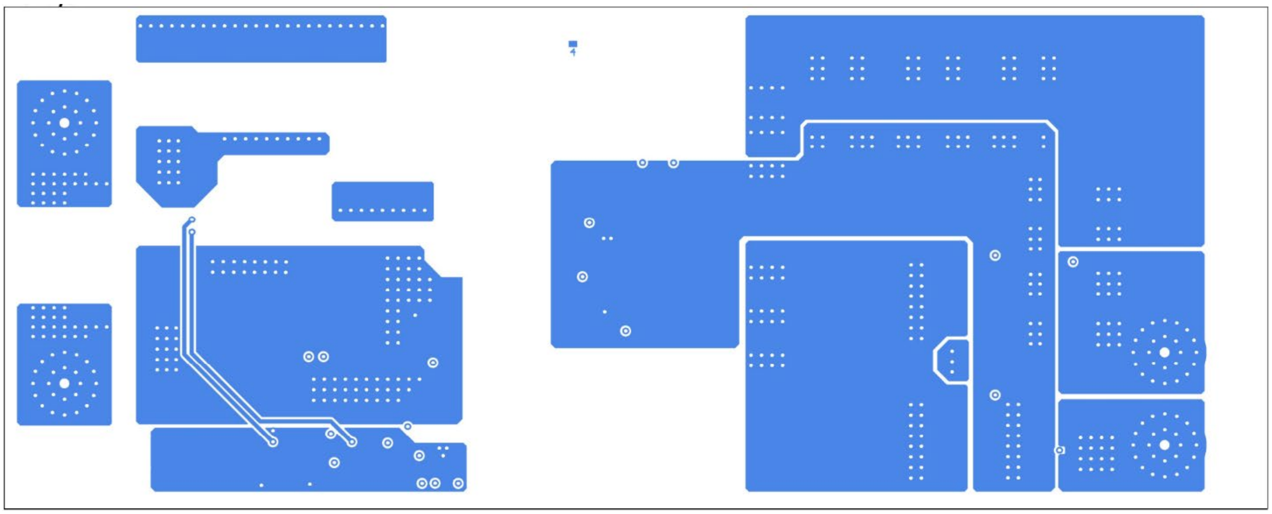


Figure 13 – DER-953Q Mid-Layer 4 PCB Layout.

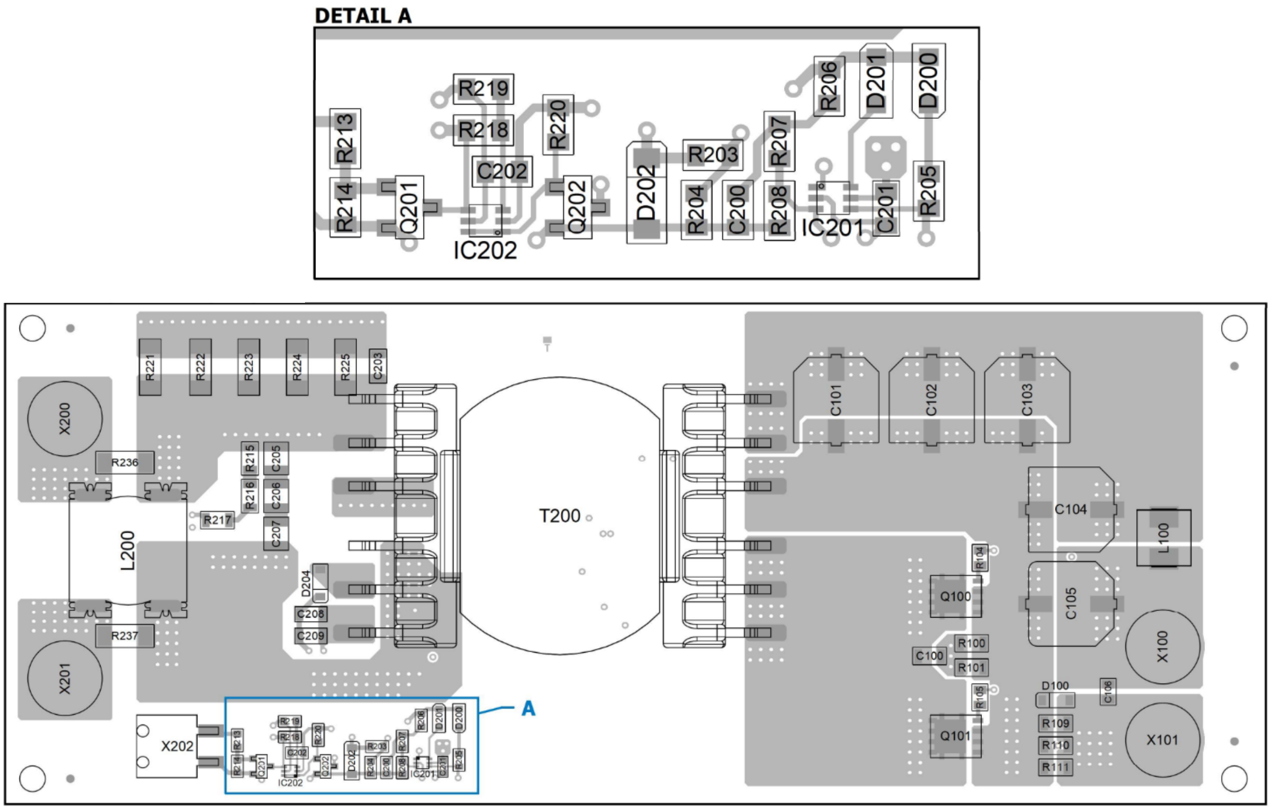


Figure 14 – DER-953Q PCB Assembly (Top).

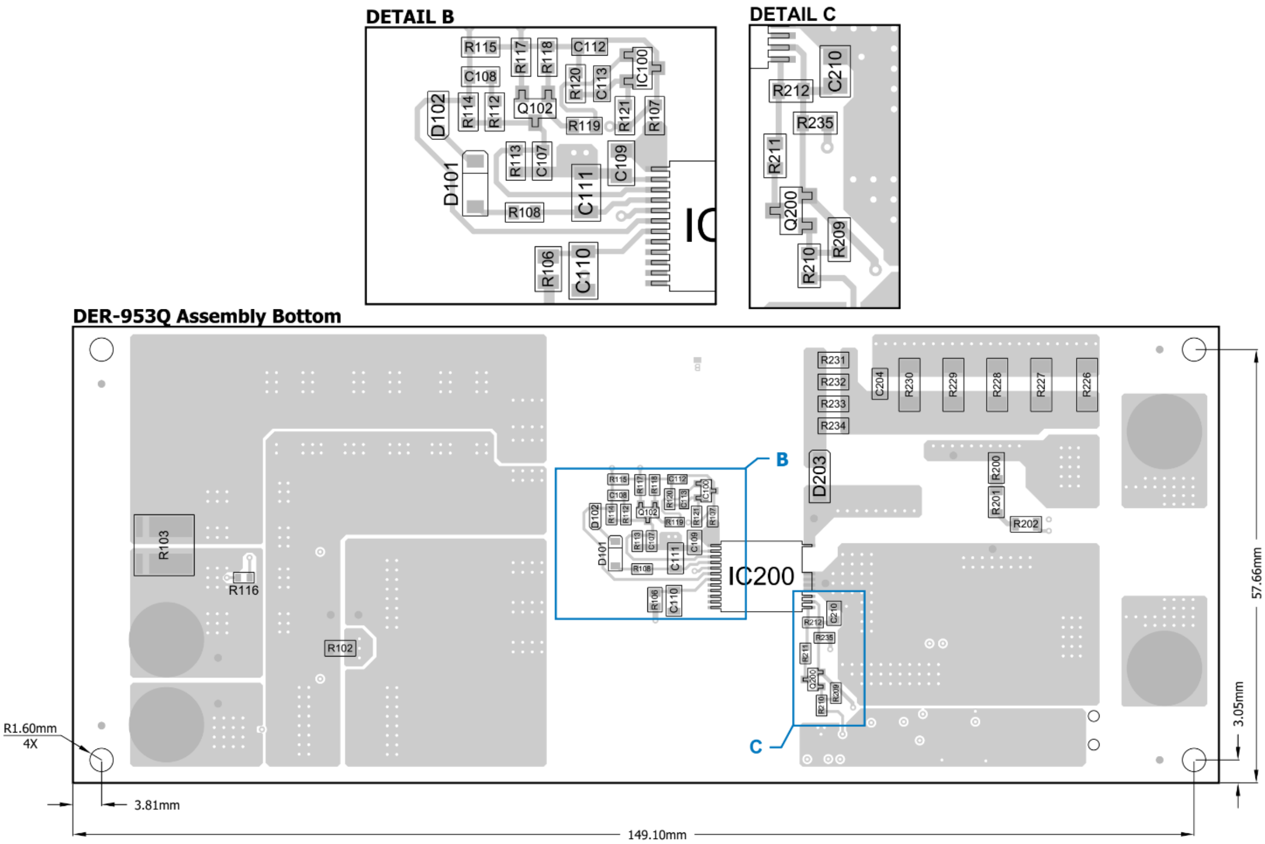


Figure 15 – DER-953Q PCB Assembly (Bottom).

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	1	C100	Ceramic Chip Capacitor 4n7 C0G 250 V 20% 1206	C1206C472MAGECAUTO	KEMET
2	4	C101, C102, C103, C104	Polymer Aluminium Capacitor 560u AL 25 V 20% 10.3 X 10.3 mm	EEH-ZU1E561P	Panasonic
3	1	C105	Polymer Aluminium Capacitor 1000u AL 25 V 20% 10.3 X 10.3 mm	EEH-ZS1E102UP	Panasonic
4	1	C106	Ceramic Chip Capacitor 2u2 X7R 35 V 10% 0805	CGA4J1X7R1V225K125AC	TDK
5	1	C107	Ceramic Chip Capacitor 220p C0G 50 V 5% 0603	CGA3E2NP01H221J080AA	TDK
6	1	C108	Ceramic Chip Capacitor 10n X7R 50 V 20% 0603	C0603C103M5RACAUTO	KEMET
7	2	C109, C210	Ceramic Chip Capacitor 4u7 X7R 16 V 20% 0805	CGA4J3X7R1C475M125AB	TDK
8	1	C110	Ceramic Chip Capacitor 330p C0G 500 V 10% 1206	C1206C331KCGACAUTO	KEMET
9	1	C111	Ceramic Chip Capacitor 2u2 X7R 25 V 20% 1206	CGA5L2X7R1E225M160AA	TDK
10	1	C113	Ceramic Chip Capacitor 27n X7R 25 V 5% 0603	C0603C273J3RACAUTO	KEMET
11	1	C200	Ceramic Chip Capacitor 470n X7R 25 V 10% 0603	CGA3E3X7R1E474K080AB	TDK
12	2	C201, C202	Ceramic Chip Capacitor 100n X7R 25 V 10% 0603	CGA3E2X7R1E104K080AA	TDK
13	2	C203, C204	Ceramic Chip Capacitor 68n X7R 250 V 10% 1206	C1206C683KARECAUTO	KEMET
14	3	C205, C206, C207	Ceramic Chip Capacitor 150n X7R 500 V 10% 1210	C1210X154KCRACAUTO	KEMET
15	2	C208, C209	Ceramic Chip Capacitor 10000p X7R 50 V 10% 1206	C1206C103K5RACAUTO	KEMET
16	1	D100	Schottky Diode 40 V 3 A SOD123W	PMEG4030ER-QX	Nexperia
17	2	D101, D202	Zener Diode 15 V 365 mW SOD123	PDZ15BGWX	Nexperia
18	2	D102, D200	Diode Standard 100 V 250 mA SOD-323	BAS16J,115	Nexperia
19	1	D201	DIODE ZENER 2.7 V 200 mW SOD-323	BZX384C2V7-HE3-08	Vishay
20	1	D203	DIODE SCHOTTKY 1KV 1A DO-214AC (SMA)	ACURA107-HF	Comchip
21	1	D204	Diode Standard 200 V 225mA (DC) Surface Mount SOD-123	BAS21GWX	Nexperia
22	1	IC100	Voltage References Automotive, high-bandwidth, low-IQ programmable shunt regulator ATL431LIBQDBZRQ1 2.5 V to 36 V SOT-23	ATL431LIBQDBZRQ1	Texas Instruments
23	1	IC200	InnoSwitch3 InSOP-24D CV/CC QR Flyback Switcher IC with Integrated 900 V Switch and FluxLink Feedback for Automotive Applications	INN3990CQ	Power Integrations
24	2	IC201, IC202	AUTOMOTIVE LOW-POWER WINDOW COMP 1.8 V to 18 V 6-WSON	TLV6700QDSERQ1	Texas Instrument
25	1	L100	Shielded Power Inductor 680 nH 7.00 mm x 6.60 mm	SRP7020TA-R68M	Bourns
26	1	L200	Input Common Mode Choke 1.4mH		
27	2	Q100, Q101	N-Channel MOSFET 120 V 90 A PowerDI5060-8	DMT12H007LPS-13[12]	Diodes
28	2	Q102, Q200	40 V 0.2 A PNP bipolar transistor 300 mW SOT-23	MMBT3906-7-F	Diodes
29	2	Q201, Q202	N-Channel MOSFET 30 V 500 mA 690 mW 1.5 Ohm @ 10 mA, 4 V SOT23	NVR4003NT3G	Onsemi
30	3	R100, R101, R102	Thick Film Chip Resistor 18R 5% 0.25W 200V 1206	RMCF1206JT18R0	Stackpole
31	2	R104, R105	Jumper Resistor 0R 0805	ERJ-6GEY0R00V	Panasonic
32	1	R106	Thick Film Chip Resistor 100R 5% 0.125W 150V 0805	RMCF0805JT100R	Stackpole
33	1	R107	Thick Film Chip Resistor 10R 5% 0.1W 75V 0603	CRGCQ0603J10R	TE
34	1	R108	Thick Film Chip Resistor 100R 5% 0.1W 0603	RMCF0603JT100R	Stackpole
35	3	R109, R110, R111	Current Sense Resistor 0R012 1% 1W 200V 1206	WSLP1206R0120FEA	Vishay
36	1	R112	Thick Film Chip Resistor 56k 5% 0.1W 150V 0603	ERJ-3GEYJ563V	Panasonic
37	1	R113	Thick Film Chip Resistor 10k2 1% 0.1W 150V 0603	RMCF0603FT10K2	Stackpole
38	1	R114	Thick Film Chip Resistor 110k 5% 0.1W 150V 0603	RMCF0603JT110K	Stackpole
39	1	R116	Jumper Resistor 0R 0603	ERJ-3GEY0R00V	Panasonic
40	1	R117	Thick Film Chip Resistor 430k 5% 0.1W 150V 0603	ERJ-3GEYJ434V	Panasonic
41	1	R118	Thick Film Chip Resistor 33k 5% 0.1W 150V 0603	RMCF0603JT33K0	Stackpole

[12] DMT12H007LPS-13 is not fully AEC-Q qualified.

42	1	R119	Thick Film Chip Resistor 11k 5% 0.1W 150V 0603	RMCF0603JT11K0	Stackpole
43	1	R120	Thick Film Chip Resistor 127k 1% 0.1W 150V 0603	ERJ-3EKF1273V	Panasonic
44	1	R121	Thick Film Chip Resistor 28k7 1% 0.1W 150V 0603	ERJ-3EKF2872V	Panasonic
45	3	R200, R201, R202	Thick Film Chip Resistor 1M 1% 0.25W 200V 1206	RMCF1206FT1M00	Stackpole
46	1	R203	Thick Film Chip Resistor 88k7 1% 0.1W 150V 0603	ERJ-3EKF8872V	Panasonic
47	1	R204	Thick Film Chip Resistor 42k2 1% 0.1W 150V 0603	ERJ-3EKF4222V	Panasonic
48	1	R205	Thick Film Chip Resistor 2M 1% 0.1W 150V 0603	RMCF0603FT2M00	Stackpole
49	1	R206	Thick Film Chip Resistor 27k 5% 0.1W 150V 0603	ERJ-3GEYJ273V	Panasonic
50	1	R207	Thick Film Chip Resistor 1M 5% 0.1W 150V 0603	ERJ-3GEYJ105V	Panasonic
51	1	R208	Thick Film Chip Resistor 100k 5% 0.1W 150V 0603	ERJ-3GEYJ104V	Panasonic
52	1	R209	Thick Film Chip Resistor 240k 5% 0.1W 150V 0603	ERJ-3GEYJ244V	Panasonic
53	1	R210	Thick Film Chip Resistor 130k 5% 0.1W 150V 0603	ERJ-3GEYJ134V	Panasonic
54	1	R211	Thick Film Chip Resistor 18k 5% 0.1W 150V 0603	ERJ-3GEYJ183V	Panasonic
55	1	R212	Thick Film Chip Resistor 47k 5% 0.1W 150V 0603	ERJ-3GEYJ473V	Panasonic
56	1	R213	Thick Film Chip Resistor 4k7 5% 0.1W 150V 0603	ERJ-3GEYJ472V	Panasonic
57	1	R214	Thick Film Chip Resistor 10k 5% 0.1W 150V 0603	ERJ-3GEYJ103V	Panasonic
58	3	R215, R216, R217	Thick Film Chip Resistor 3M 1% 0.25W 200V 1206	RMCF1206FT3M00	Stackpole
59	1	R218	Thick Film Chip Resistor 21k 1% 0.1W 100V 0603	ERJ-3EKF2102V	Panasonic
60	1	R219	Thick Film Chip Resistor 6k8 1% 0.1W 150V 0603	ERJ-3EKF6801V	Panasonic
61	1	R220	Thick Film Chip Resistor 51k 5% 0.1W 150V 0603	ERJ-3GEYJ513V	Panasonic
62	10	R221, R222, R223, R224, R225, R226, R227, R228, R229, R230	MELF Resistors 82k 1% 1W 200V MELF 0207	MMB02070C8202FB200	Vishay
63	4	R231, R232, R233, R234	Thick Film Chip Resistor 82R 5% 0.25W 200V 1206	RMCF1206JT82R0	Stackpole
64	1	R235	Thick Film Chip Resistor 15k 5% 0.1W 150V 0603	ERJ-3GEYJ153V	Panasonic
65	1	T200	100W Power Transformer		Power Integrations
66	2	T200-Core	SSP-95A POT/3319 Ferrite Core		Sunshine
67	1	T200-Bobbin	Customized bobbin	MCT-POT3301	Power Integrations
68	4	X100, X101, X200, X201	1 Pin Screw Terminal, Power Tap M5 SMT 7466105R 70A	7466105R	Würth
69	1	X202	TERMI-BLOK SMT 180_2P_3.81 2383945-2 12A 1x2Pin, Pitch 3.81mm	2383945-2	TE

Table 4 – DER-953Q Bill of Materials[13].

[13] All components are AEC-Q qualified except the SR MOSFET, connectors, and transformer.

7 Transformer Specification (T200)

7.1 Electrical Diagram

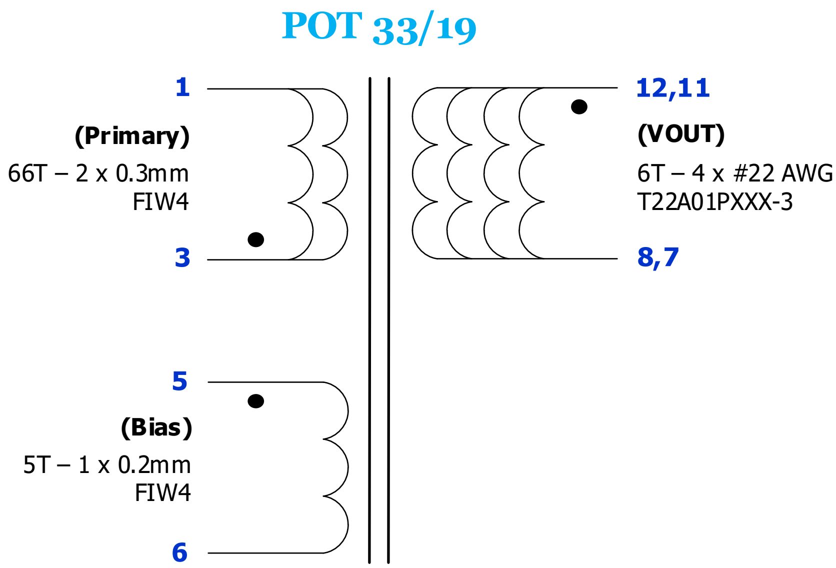


Figure 16 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			100	W
Input voltage Vdc	Flyback topology	40	380	500	V
Switching frequency	Flyback topology			43	kHz
Duty cycle	Flyback topology	51.8		71.2	%
Np:Ns			11		
Rdc	Primary side		536		mΩ
Rdc	Secondary side		5.8		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency between pin 3 and pin 7, with pins 5-6 shorted, pins 1-3 shorted and pins 7-8-11-12 shorted at 25°C		160		pF
Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 3, with all other windings open at 25 °C		1277		µH
Part to part tolerance	Tolerance of Primary Inductance		3		%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.		10		µH

Table 5 – Transformer (T1) Electrical Specifications.

7.3 Transformer Build Diagram

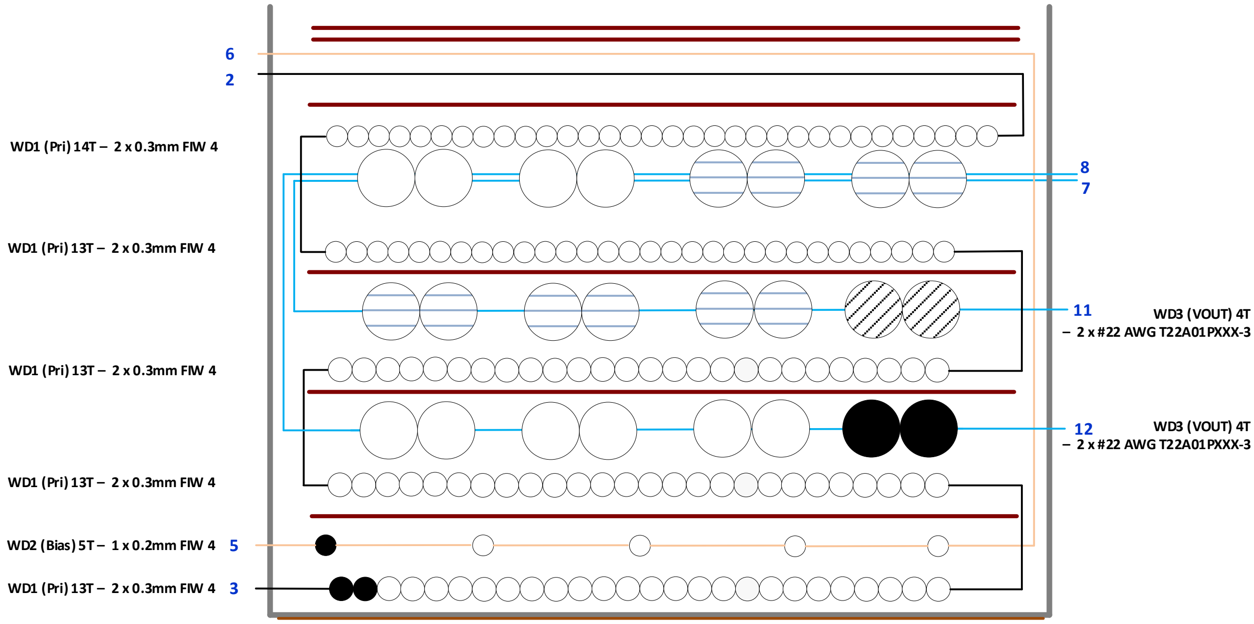


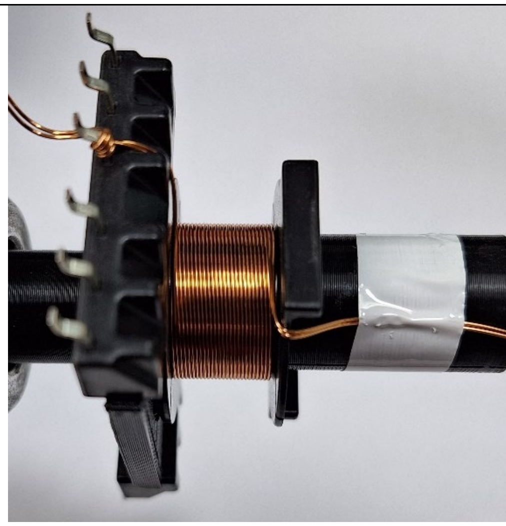
Figure 17 – Transformer Build Diagram.

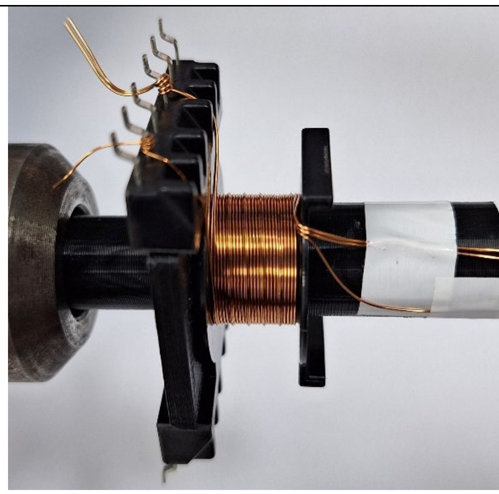
7.4 Material List

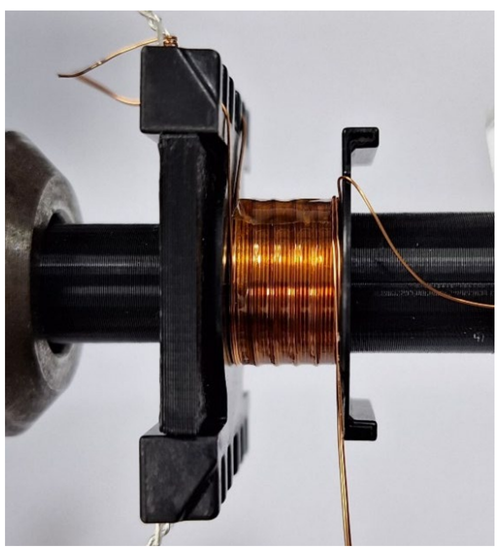
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: MCT-POT3301	1	PC	Phenolic	MyCoilTech
[2]	Core: POT33/19	2	PCS	SSP-95A (or equivalent)	Sunshine
[3]	WD1 (Pri): 0.30 mm FIW 4, Class F		mm	Copper Wire	Elektrisola
[4]	WD2 (Bias): 0.20 mm FIW 4, Class F		mm		Elektrisola
[5]	WD3 (VOUT): T22A01PXXX-3, AWG 22 PFA .003”		mm		Rubadue
[5]	3M Polyimide Film Tape 5413, width: 0.38in (9.65mm)		mm	3M 5413 0.38" X 36YD (or equivalent)	3M

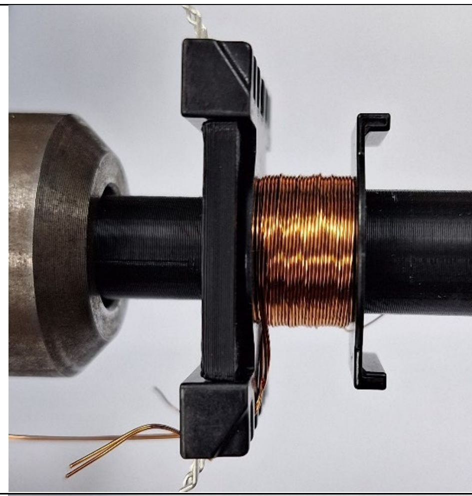
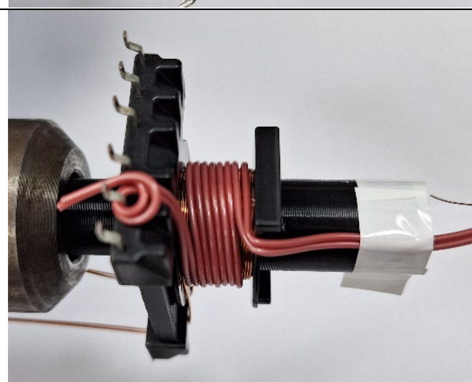
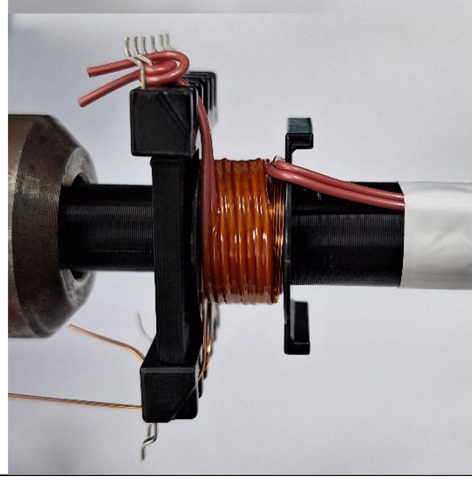
Table 6 – Transformer (T200) Material List.

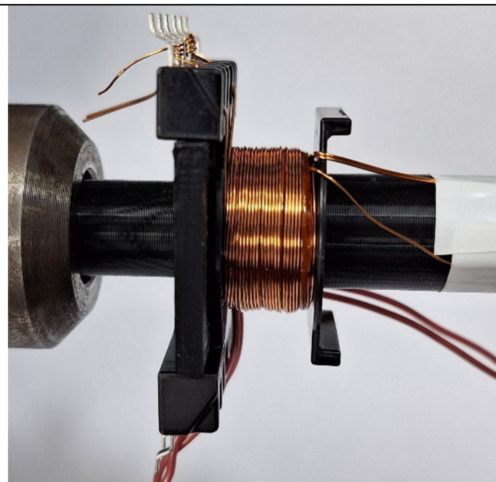
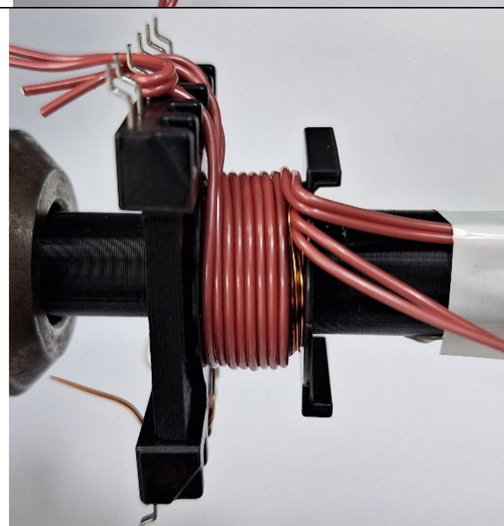
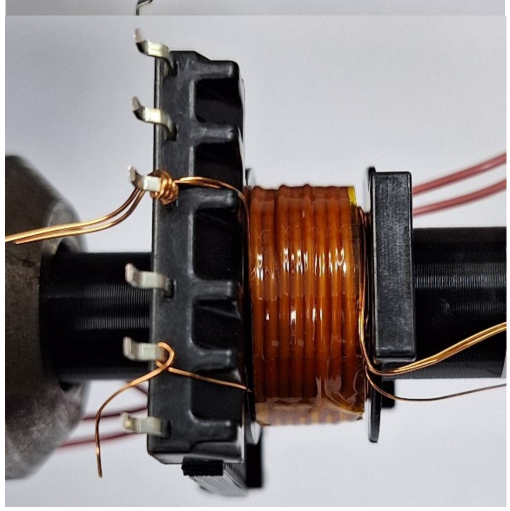
7.5 Winding Instructions

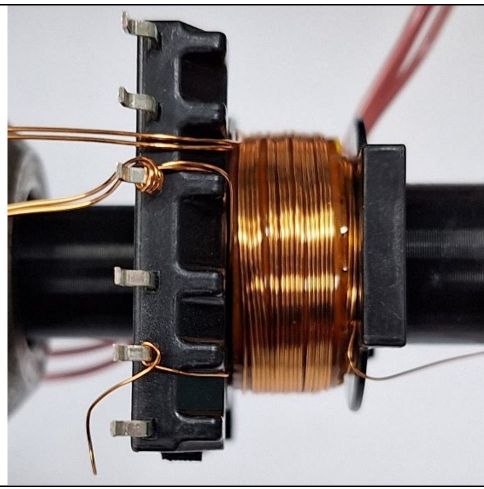
<table>
<tr><td>WD1 (Pri)</td><td></td><td>Use 2x0.3mm FIW4 wire.
Start on PIN 3.

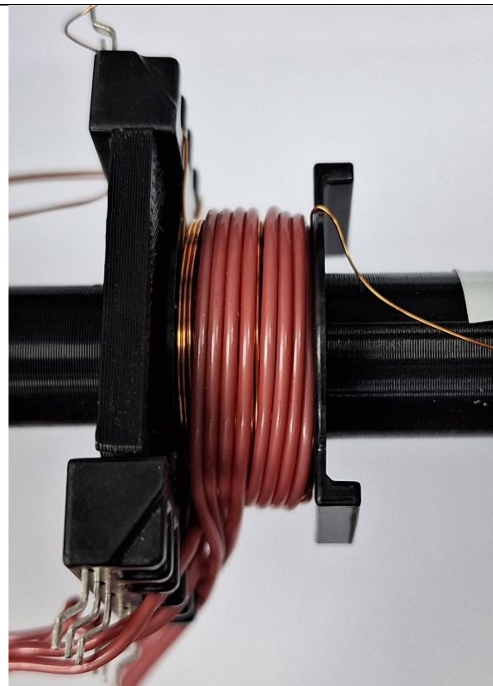
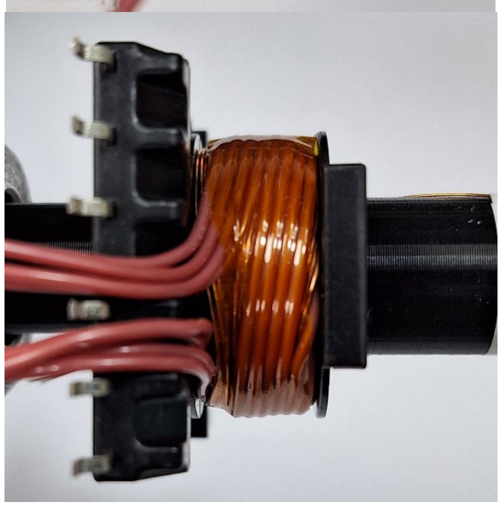
Wind the primary winding's first layer, 13 turns from left to right. Spread the winding evenly along the bobbin's width.
Do not terminate yet.</td></tr>
<tr><td rowspan="2">WD2 (Bias)</td><td></td><td>Use 0.2mm FIW4 wire.
Start on PIN 5.

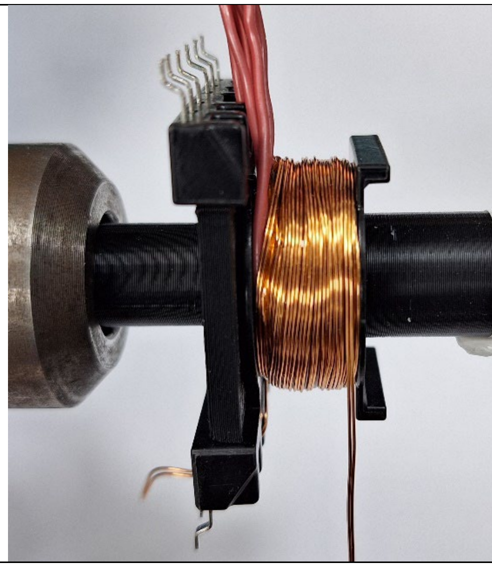
Wind the bias winding,
5 turns from left to right.
Spread the winding evenly along the bobbin's width.
Do not terminate yet.</td></tr>
<tr><td></td><td>Secure using 1 Layer of tape.</td></tr>
</table>

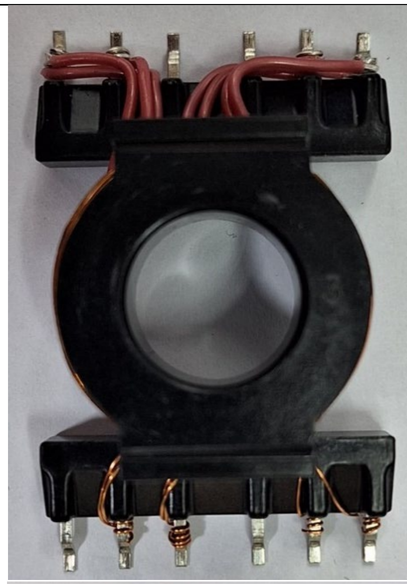
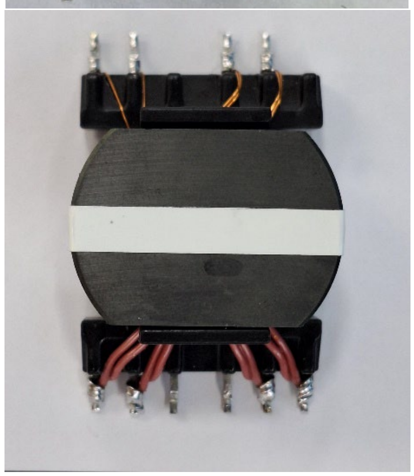
WD1 (Pri)		Continue winding the primary wire. Wind the primary winding's second layer, 13 turns from right to left. Spread the winding evenly along the bobbin's width. Do not terminate yet.
WD3 (VOUT)	 	Use 2 x #22 AWG T22A01PXXX-3. Start on PIN 12. Wind the secondary winding's first layer, 4 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet. Secure using 1 Layer of tape.

WD1 (Pri)		Continue winding the primary wire. Wind the primary winding's third layer, 13 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.
WD3 (VOUT)	 	Use another 2 x #22 AWG T22A01PXXX-3. Start on PIN 11 Wind the additional secondary winding layer, 4 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet. Secure using 1 Layer of tape.

WD1 (Pri)		Continue winding the primary wire. Wind the primary winding's fourth layer, 13 turns from right to left. Spread the winding evenly along the bobbin's width. Do not terminate yet.

WD3 (VOUT)	 	Continue winding the secondary wire. Combining the 4 wires of the secondary winding, wind 2 turns from right to left. Spread the winding evenly along the bobbin's width. Secure using 1 Layer of tape.

WD1 (Pri)		Continue winding the primary wire. Wind the primary winding's fifth layer, 14 turns from left to right. Spread the winding evenly along the bobbin's width. Secure using 2 Layers of tape. Terminate primary winding at PIN 2.
WD2 (Bias)		No additional turns. Terminate bias winding at PIN 6 by laying it flat across the bobbin's width. Secure using 1 Layer of tape.

Finishing	 	Terminate secondary winding at PIN 7 and 8. *PIN 7 and 8 can be interchanged since they are shorted on the PCB* Cut wires. Mount the gapped core using glue (a polyester film electrical tape can be used as alternative) Remove pins 1 and 4.

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VOUT	13.50		13.50	V	Output Voltage
4	OPERATING CONDITION 1					
5	VINDC1	500.00		500.00	V	Input DC voltage 1
6	IOUT1	7.350		7.350	A	Output current 1
7	POUT1			99.23	W	Output power 1
8	EFFICIENCY1	0.93		0.93		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	OPERATING CONDITION 2					
12	VINDC2	140.00		140.00	V	Input DC voltage 2
13	IOUT2	7.350		7.350	A	Output current 2
14	POUT2			99.23	W	Output power 2
15	EFFICIENCY2	0.95		0.95		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	PRIMARY CONTROLLER SELECTION					
70	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
71	VDRAIN_BREAKDOWN	900		900	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X0		Device selection
73	DEVICE_CODE	INN3990CQ		INN3990CQ		Device code
74	PDEVICE_MAX			100	W	Device maximum power capability
75	RDSON_25DEG			0.39	Ω	Primary switch on-time resistance at 25°C
76	RDSON_125DEG			0.65	Ω	Primary switch on-time resistance at 125°C
77	ILIMIT_MIN			2.395	A	Primary switch minimum current limit
78	ILIMIT_TYP			2.576	A	Primary switch typical current limit
79	ILIMIT_MAX			2.756	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.47	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			678	V	Peak drain voltage on the primary switch during turn-off
85	WORST CASE ELECTRICAL PARAMETERS					
86	FSWITCHING_MAX	43000		43000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	148.0		148.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			0.633		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			CCM		Mode of operation

90	DUTYCYCLE			0.515		Primary switch duty cycle
91	TIME_ON_MIN			5.07	us	Minimum primary switch on-time
92	TIME_ON_MAX		Info	19.19	us	Maximum primary switch on-time is greater than 11.75us: Increase the controller switching frequency or increase the VOR
93	TIME_OFF			11.29	us	Primary switch off-time
94	LPRIMARY_MIN			1238.8	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			1277.2	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	3.0		3.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			1315.5	uH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			0.730	A	Primary switch average current
101	IPEAK_PRIMARY			2.257	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.762	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			2.231	A	Primary switch ripple current
104	IRMS_PRIMARY			1.075	A	Primary switch RMS current
108	**TRANSFORMER CONSTRUCTION PARAMETERS**					
109	**CORE SELECTION**					
110	CORE	POT33		POT33		Core selection
111	CORE NAME			POT33/19		
112	AE			150.0	mm^2	Core cross sectional area
113	LE			51.4	mm	Core magnetic path length
114	AL			7500	nH	Ungapped core effective inductance per turns squared
115	VE			7710	mm^3	Core volume
116	BOBBIN NAME	POT33/19		POT33/19		Bobbin name
117	AW	49.3		49.3	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW	10.50		10.50	mm	Bobbin width
119	BH	4.69		4.69	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
122	**PRIMARY WINDING**					
123	NPRIMARY			66		Primary winding number of turns
124	BPEAK			3748	Gauss	Peak flux density
125	BMAX			2967	Gauss	Maximum flux density
126	BAC			1464	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			293	nH	Typical gapped core effective inductance per turns squared
128	LG			0.618	mm	Core gap length
130	**SECONDARY WINDING**					
131	NSECONDARY	6		6		Secondary winding number of turns
133	**BIAS WINDING**					
134	NBIAS			5		Bias winding number of turns

138	**PRIMARY COMPONENTS SELECTION**					
161	**BIAS WINDING**					
162	VBIAS			9.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			46.88	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	uF	Bias winding rectification capacitor
166	CBPP			4.70	uF	BPP pin capacitor
170	**SECONDARY COMPONENTS SELECTION**					
171	**FEEDBACK COMPONENTS**					
172	RFB_UPPER[14]			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
173	RFB_LOWER			10.20	kΩ	Lower feedback resistor
174	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
178	**MULTIPLE OUTPUT PARAMETERS**					
179	OUTPUT 1					
180	VOUT1			13.50	V	Output 1 voltage
181	IOUT1			7.350	A	Output 1 current
182	POUT1			99.23	W	Output 1 power
183	IRMS_SECONDARY1			11.482	A	Root mean squared value of the secondary current for output 1
184	IRIPPLE_CAP_OUTPUT1			8.821	A	Current ripple on the secondary waveform for output 1
185	NSECONDARY1			6		Number of turns for output 1
186	VREVERSE_RECTIFIER1			58.95	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
187	SRFET1	DMT12H007LPS-13		DMT12H007LPS-13		Secondary rectifier (Logic MOSFET) for output 1
188	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
189	VBREAKDOWN_SRFET1			120	V	SRFET breakdown voltage for output 1
190	RDSON_SRFET1			14	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
218	PO_TOTAL			99.23	W	Total power of all outputs

Table 7 – DER-953Q PIXls Spreadsheet.

[14] Actual value implemented on the unit is 110 kΩ as requirement for implementing the *Precision Voltage Regulator* circuit.

9 Performance data

Note: 1. Measurements were taken with the unit under test set-up inside a thermal chamber placed inside a high-voltage (HV) room.

Figure 18 – High-Voltage Test Set-up.

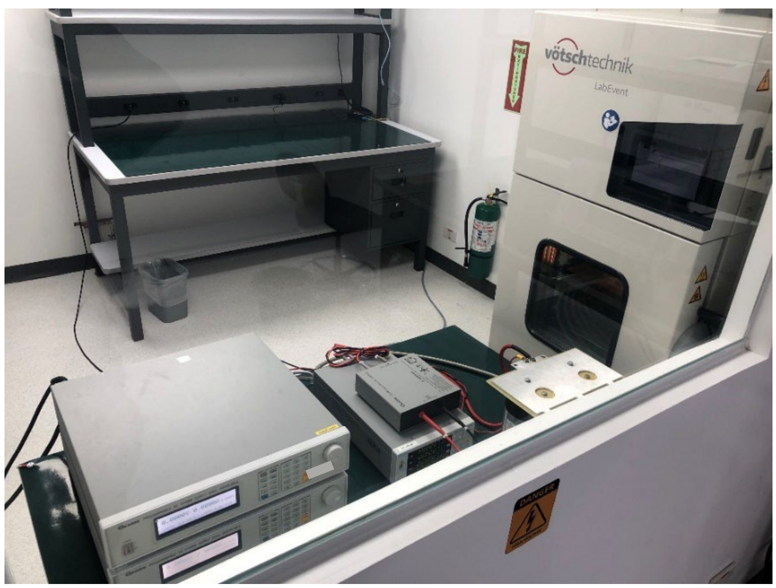


Figure 19 – Test Set-up Inside the High-Voltage Room.

2. Unit under test was placed under a box inside the thermal chamber to eliminate the effects of any airflows.

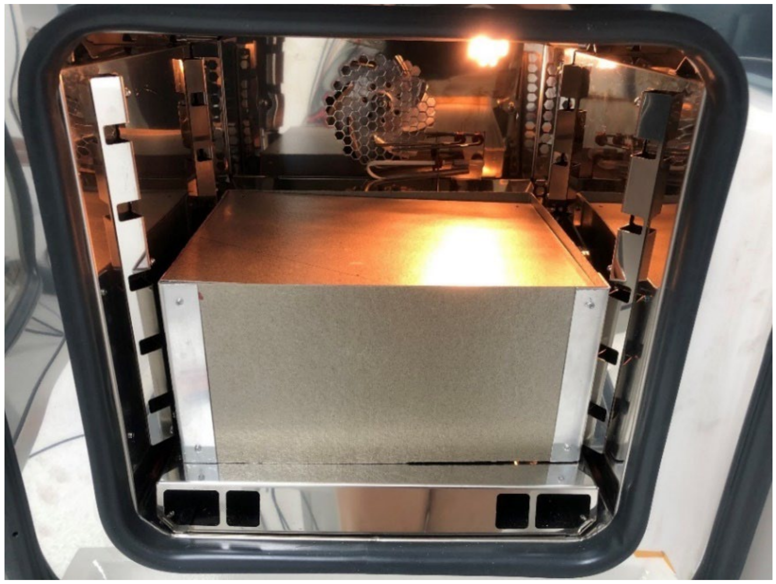


Figure 20 – Unit Under Test Placed Under a Box to Eliminate the Effect of Airflow.

3. Unit under test was soaked for 5 minutes at full load condition with every change in the input voltage during the start of every test sequence. The unit under test was soaked for at least 1 min for every loading condition before measurements were taken.
4. The following data were taken without L200 (common mode choke)
5. List of Equipment Used for Testing

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	62024P-600-8	600 V/8 A/2400 W DC PSU	Chroma
Electronic Load	DL3021	150 V/40A/200W DC ELOAD	Rigol
Electronic Load	PEL-2020A	80V/20A/100W DC ELOAD	GW Instek
Power Meter	66205	600 V/30A 10kHz Digital Meter	Chroma
Power Meter	WT310E	600 V/20 A 100kHz Digital Meter	Yokogawa
Current Meter	DMM-4050	Precision Multimeter	Tektronix
High Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Output Current Measurement	701928	100 MHz 30 A_{rms} Current Probe	Yokogawa
Component Current Measurement	CWTUM/015/B	30 MHz 30 A_{peak} Rogowski Coil	CWT
Component Current Measurement	CWTUM/06/R	30 MHz 120 A_{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20 channel Data Logger	Graphtec
Thermal Image	TiX580	1000°C Thermal Imagin Camera	Fluke
Oscilloscope	DLM5058	2.5GS/s 500MHz Mixed Signal	Yokogawa
Power Supply	62024P-600-8	600 V/8 A/2400 W DC PSU	Chroma

Table 8 – List of Equipment Used for Testing.

9.1 No-Load Input Power

Figure 21 shows the test set-up diagram for no-load input current acquisition. The voltage measuring point is placed before the ammeter; this is done to prevent the voltage-sensing bias current from affecting the input current measurement. The ammeter used was a Tektronix DMM 4050 6-1/2 Digit Precision Multimeter.

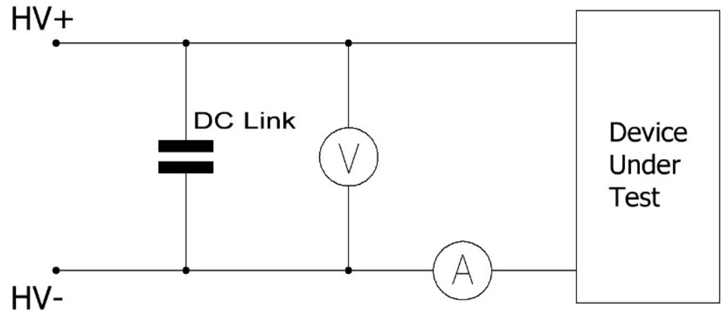


Figure 21 – No-Load Input Power Measurement Diagram.

The unit was soaked for ten minutes for every change in input voltage before starting data averaging over five minutes. Analog filtering is also enabled to improve measurement accuracy.

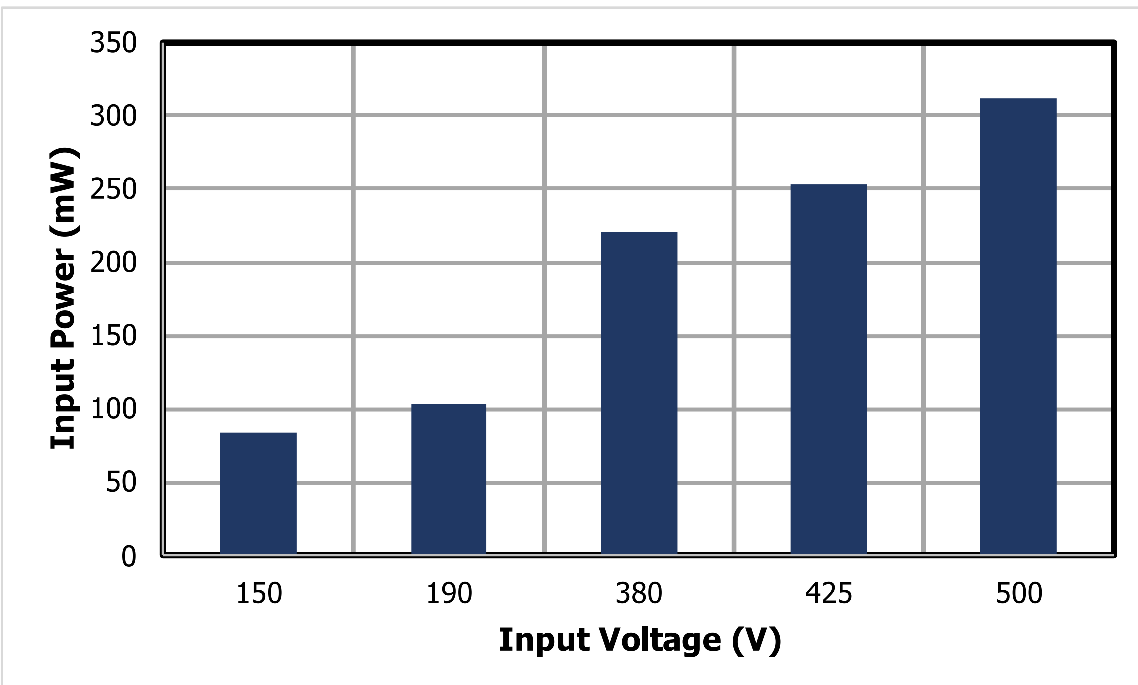


Figure 22 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

9.2 Efficiency

9.2.1 Line Efficiency

Line efficiency describes how the input voltage change affects the unit's overall efficiency. The points in the graph are only taken from 100% load conditions.

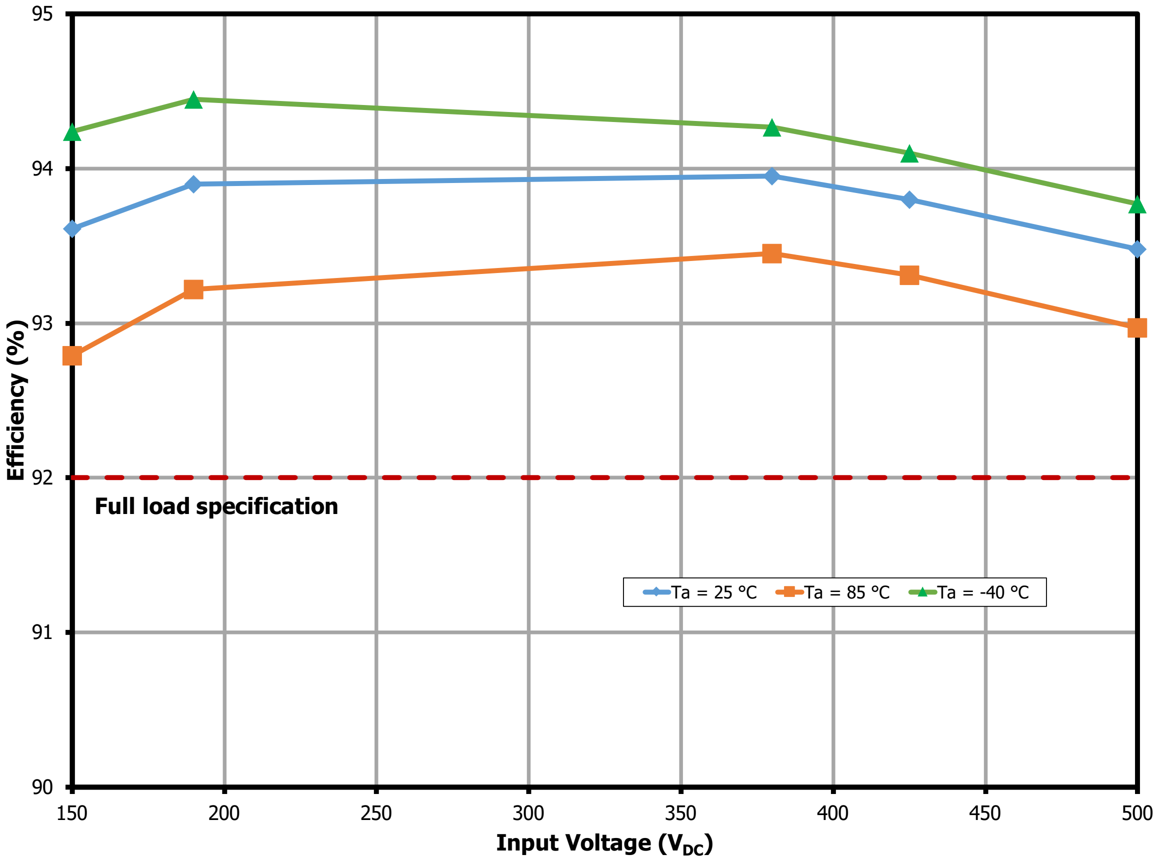


Figure 23 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the unit's overall efficiency.

9.2.2.1 Load Efficiency at 85 °C Ambient

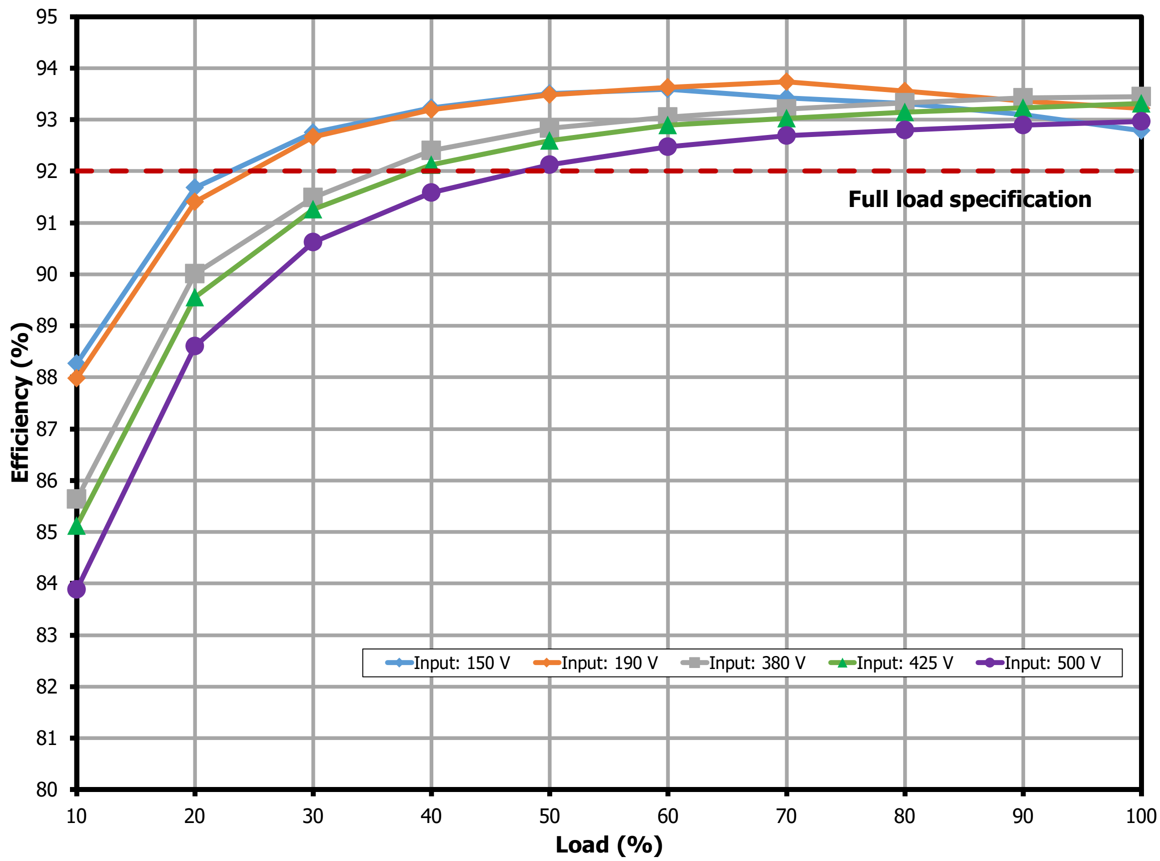


Figure 24 – Efficiency vs. Load at Different Input Voltages (85 °C Ambient).

9.2.2.2 Load Efficiency at -40 °C Ambient

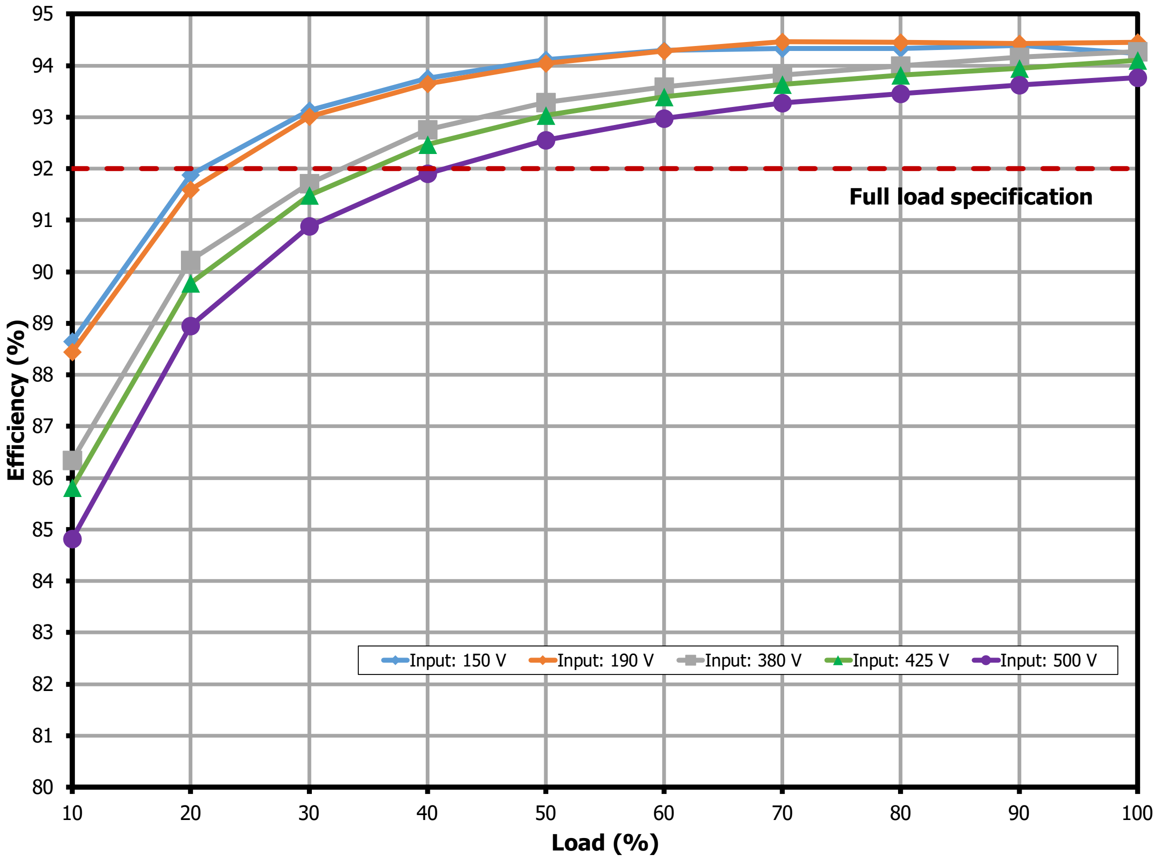


Figure 25 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

9.2.2.3 Load Efficiency at 25 °C Ambient

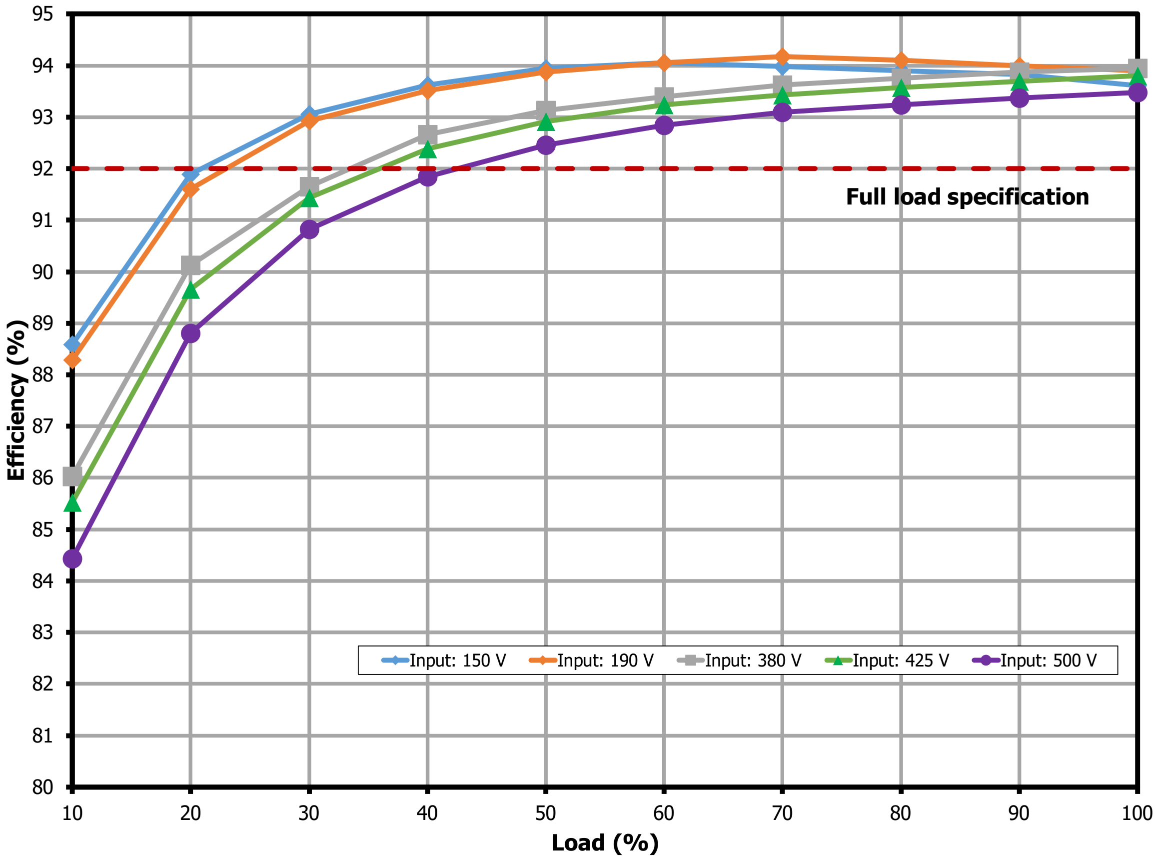


Figure 26 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

9.3 Output Line and Load Regulation

9.3.1 Load Regulation

Load Regulation describes how the change in output loading conditions affects the average output voltage of the unit.

9.3.1.1 Load Regulation at 85 °C Ambient

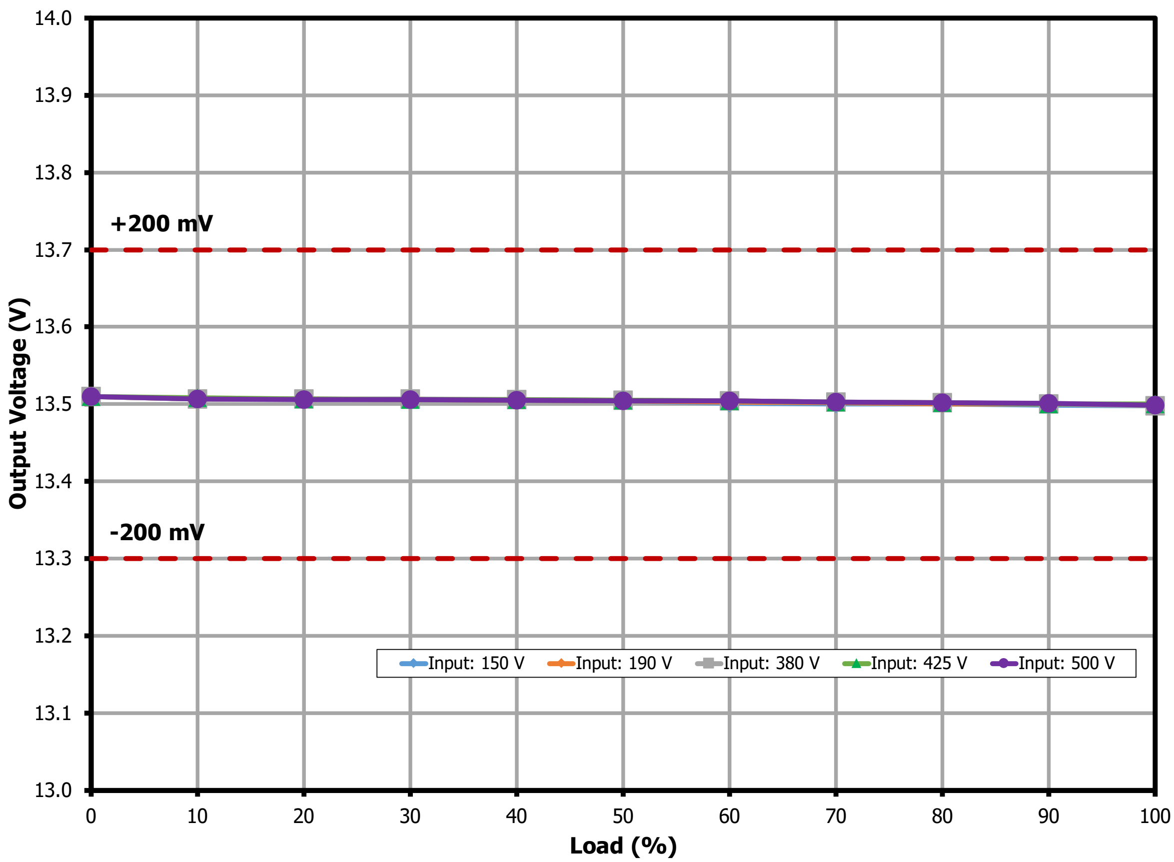


Figure 27 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).

9.3.1.2 Load Regulation at -40 °C Ambient

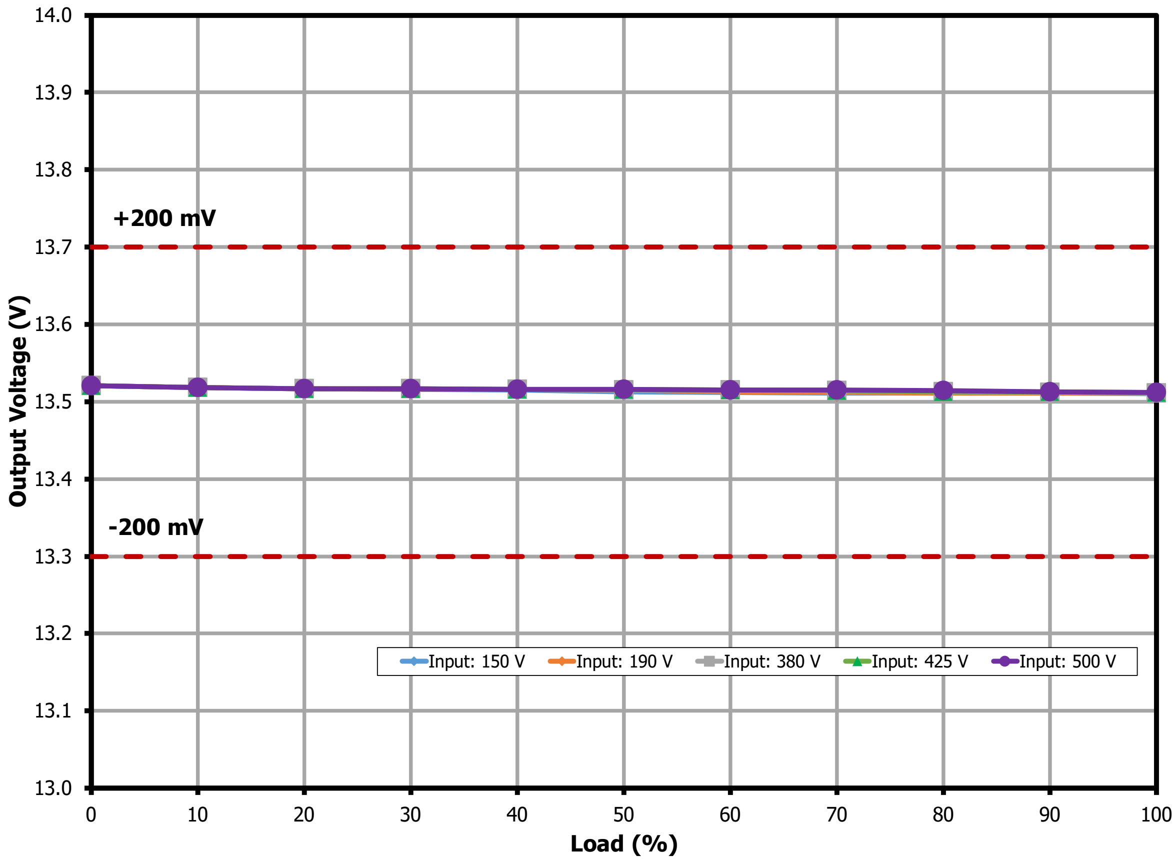


Figure 28 – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).

9.3.1.3 Load Regulation at 25 °C Ambient

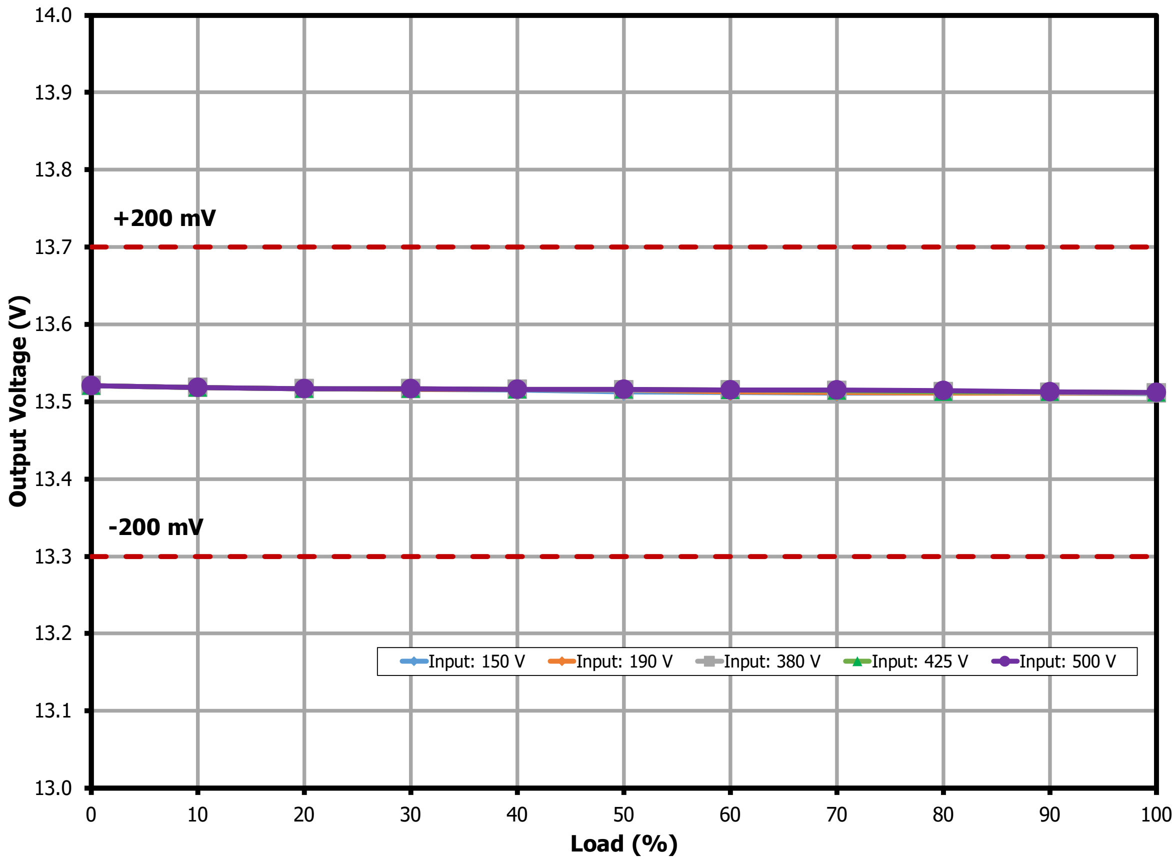


Figure 29 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).

9.3.2 Line Regulation

Line Regulation describes how the change in input voltage conditions affects the average output voltage of the unit. The points in the following graph are only taken from 100% load conditions.

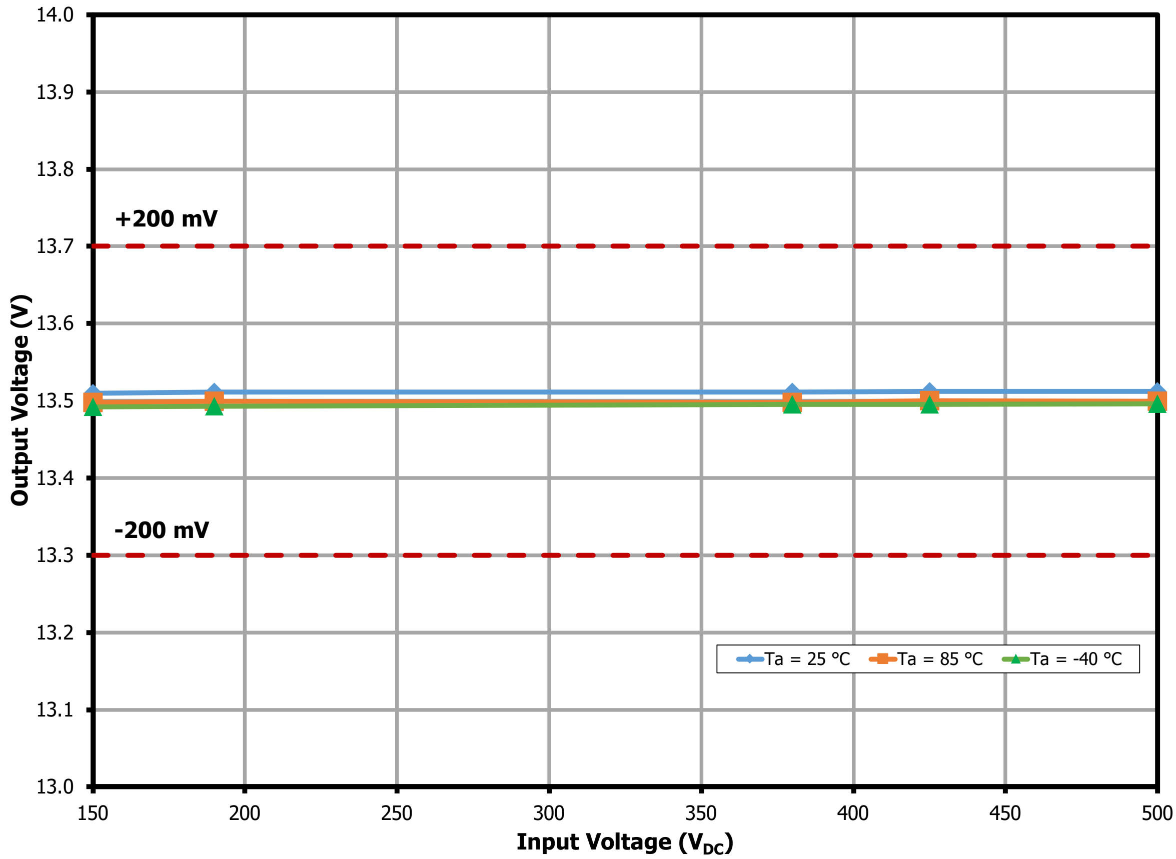


Figure 30 – Output Voltage vs Input Voltage at Full Load.

10 Thermal Performance

10.1 Thermal Data at 85 °C Ambient Temperature

The unit was placed inside a thermal chamber and soaked for at least 1 hour to allow component temperatures to settle. Figure 20 shows the set-up for thermal measurement.

Critical Components	Input Voltage		
	150	380	500
InnoSwitch3- AQ (IC200A)	124.3	112.9	116.6
Primary Snubber Resistor (R228)	117.6	112.8	112.8
Damping Resistor (R231)	119.3	111.8	111.6
Primary Snubber Diode (D203)	117.7	110.3	110.8
Transformer Core	127.6	125.5	128.3
Transformer Winding	135.3	131.3	134
Output Capacitor (C101)	106.1	103.8	105
Output Filter Inductor (L100)	111.5	109.9	111.1
Output Filter Capacitor (C105)	103.4	101.7	102.9
Synchronous Rectifier MOSFET 1 (Q100)	116.4	113.1	115.2
Synchronous Rectifier MOSFET 2 (Q101)	114.8	111.7	113.7
Secondary Snubber Resistor (R101)	111.8	110	113.6
Output Current Sense Resistor (R110)	107.3	105.9	107.3

Table 9 – Thermal Data at 85 °C at Different Input Voltages (°C).

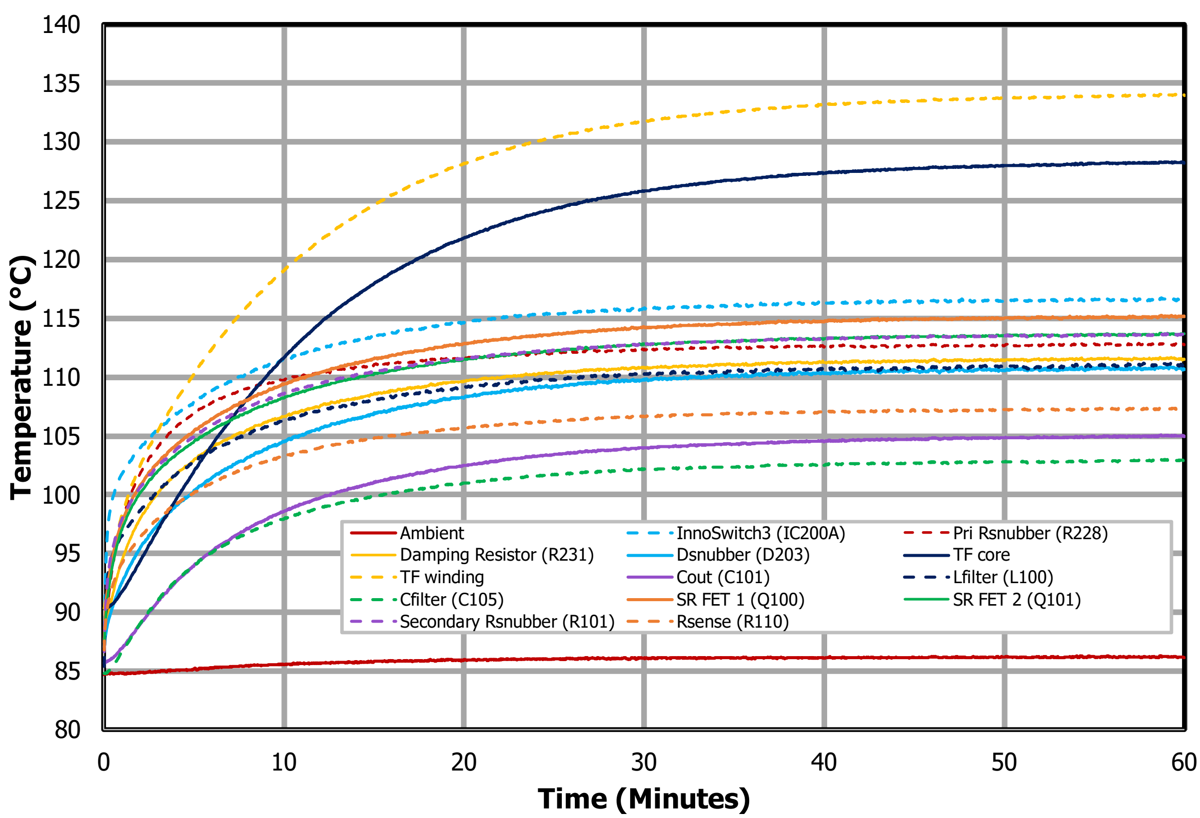


Figure 31 – Component Temperatures at 85 °C Ambient, 500 V Input.

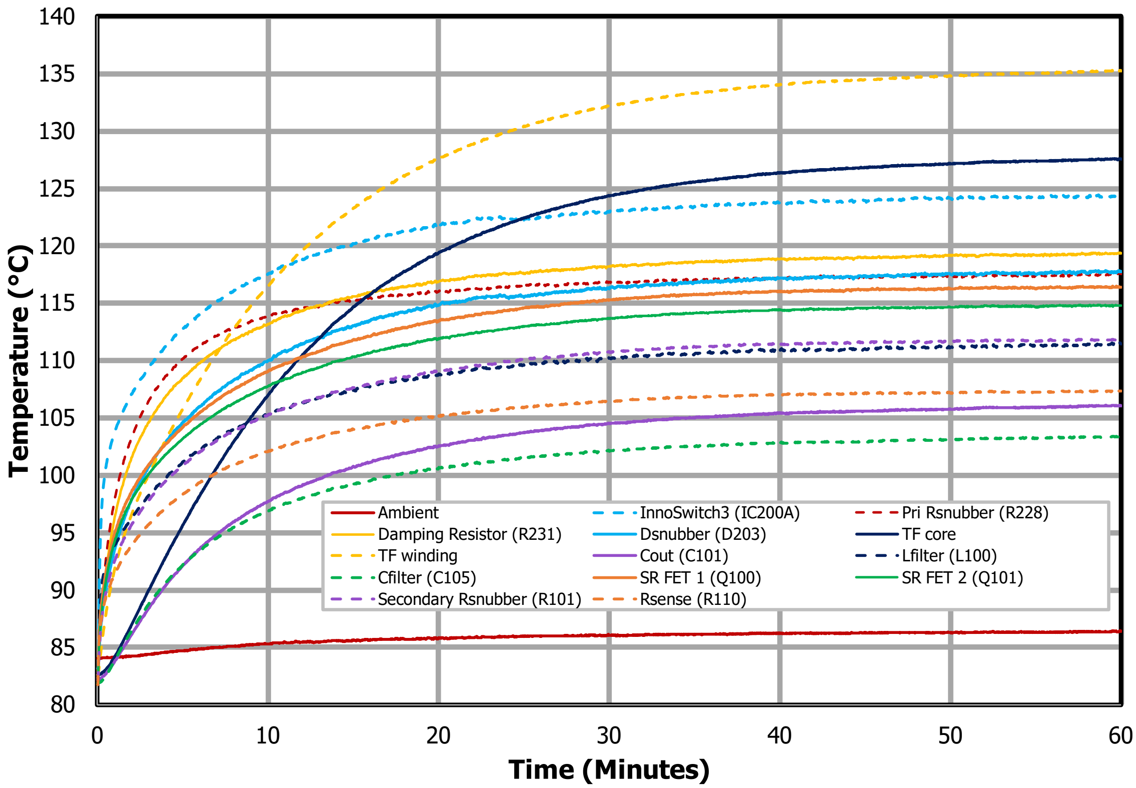


Figure 32 – Component Temperatures at 85 °C Ambient, 150 V Input.

10.2 Thermal Image Data at 23°C Room Temperature

The following thermal scans are captured using a Fluke thermal imager after soaking for at least 1 hour. The set-up is inside an enclosure to minimize the effect of airflow.

Critical Components	Input Voltage		
	150 V	380 V	500 V
InnoSwitch3- AQ (IC200A)	72.5	62.4	67.4
Primary Snubber Resistor (R228)	72.1	65.6	66.5
Damping Resistor (R231)	65.4	58.3	57.3
Primary Snubber Diode (D203)	64.8	57.8	57.4
Transformer Core	69.2	69.2	72.9
Transformer Winding	66.2	65.4	68.1
Output Capacitor (C101)	48.2	46.8	50.1
Output Filter Inductor (L100)	55.8	55.7	57.0
Output Filter Capacitor (C105)	47.2	43.6	45.4
Synchronous Rectifier MOSFET 1 (Q100)	57.5	56.0	58.6
Synchronous Rectifier MOSFET 2 (Q101)	55.3	54.4	56.7
Secondary Snubber Resistor (R101)	54.5	54.1	59.7
Output Current Sense Resistor (R110)	47.5	47.3	49.4

Table 10 – Thermal Data at 23 °C at Different Input Voltages (°C).

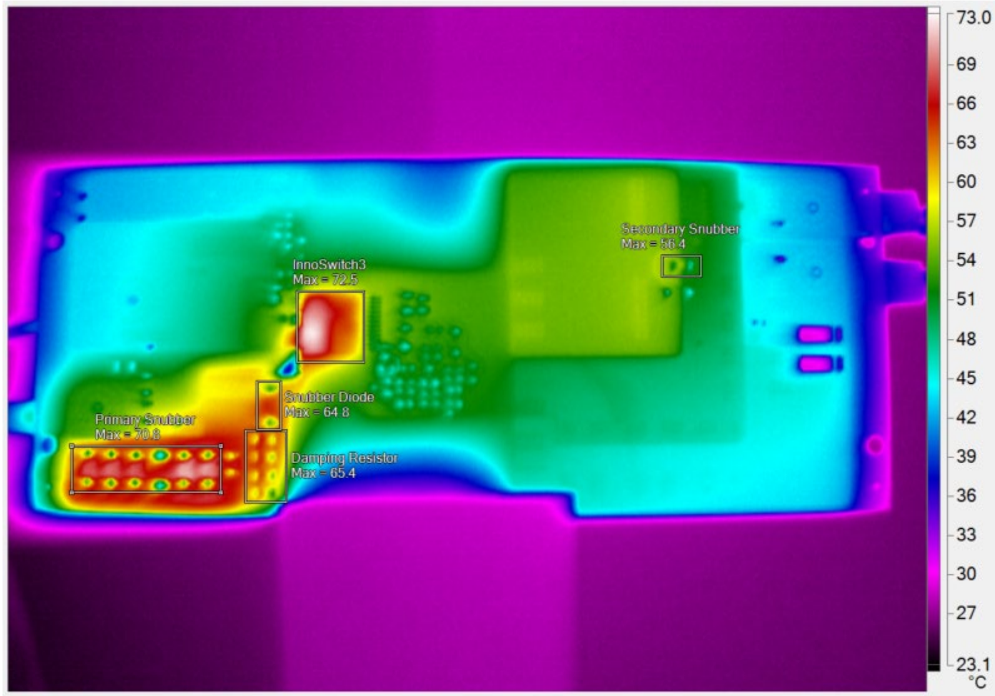


Figure 33 – PCB Bottom Thermal Scan at 150 V Input.

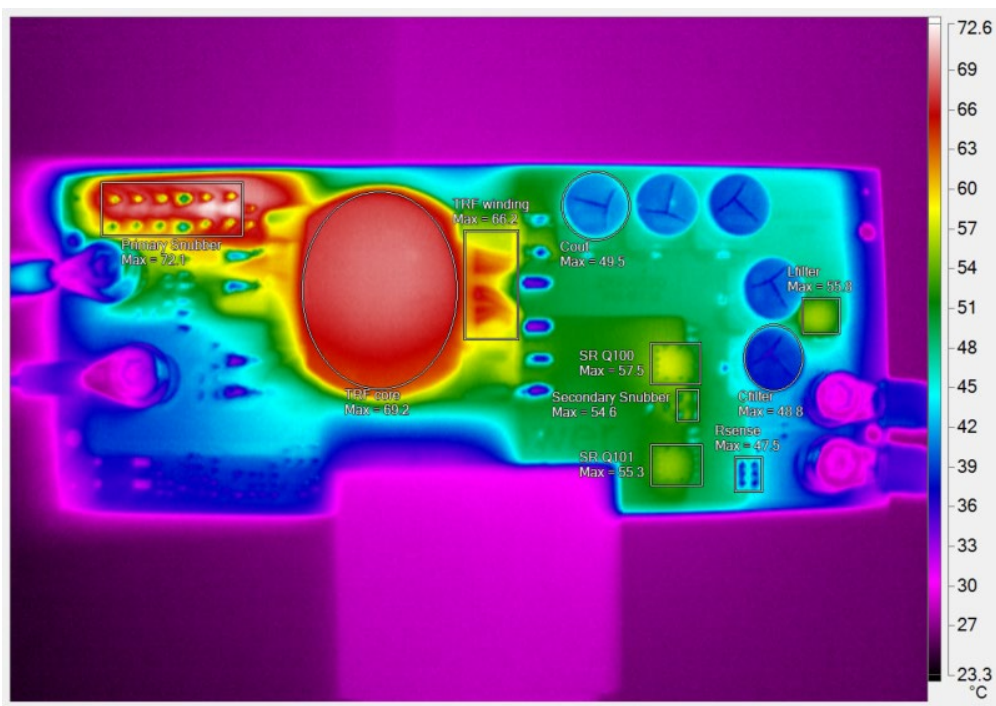


Figure 34 – PCB Top Thermal Scan at 150 V Input.

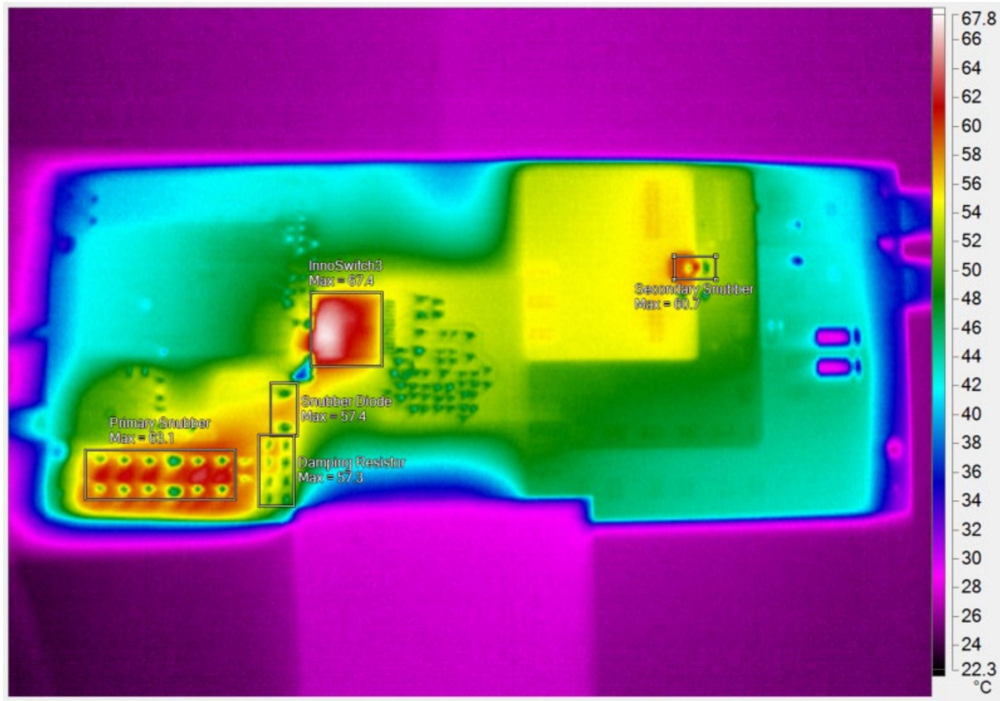


Figure 35 – PCB Bottom Thermal Scan at 500 V Input.

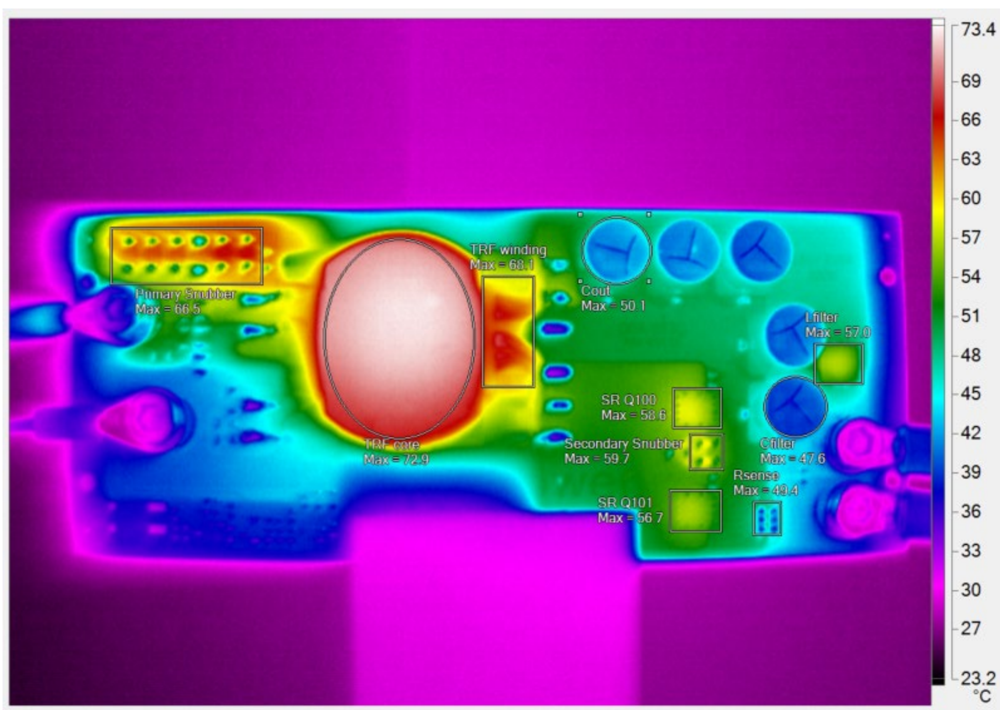


Figure 36 – PCB Top Thermal Scans at 500 V Input.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by connecting the unit under test to a fully charged DC link capacitor[15] at different test input voltages. An electronic load configured for constant resistance was used for all start-up tests.

11.1.1 Output Voltage and Current at 85 °C Ambient Temperature[16,17]

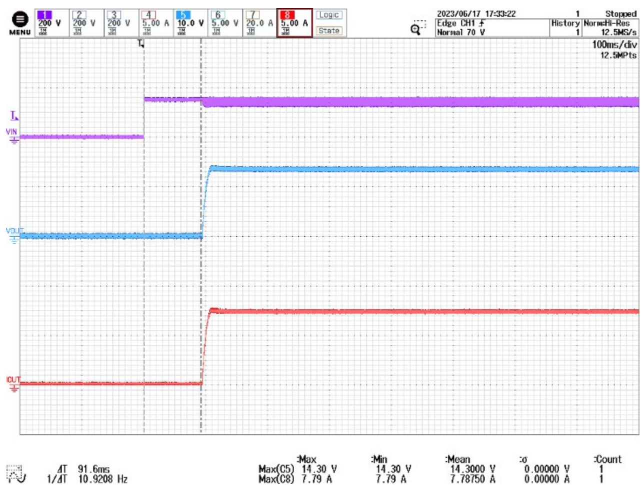


Figure 37 – Output Voltage and Current.
150 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 200 V / div.
CH5: V_{OUT}, 10 V / div.
CH8: I_{OUT}, 5 A / div.
Time: 100 ms / div.

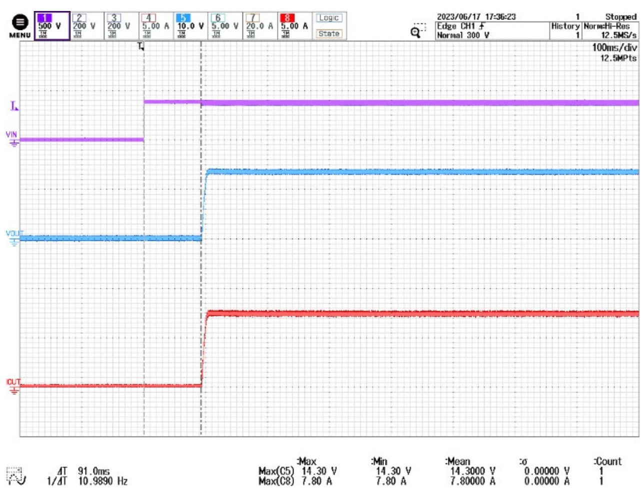


Figure 38 – Output Voltage and Current.
380 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH5: V_{OUT}, 10 V / div.
CH8: I_{OUT}, 5 A / div.
Time: 100 ms / div.

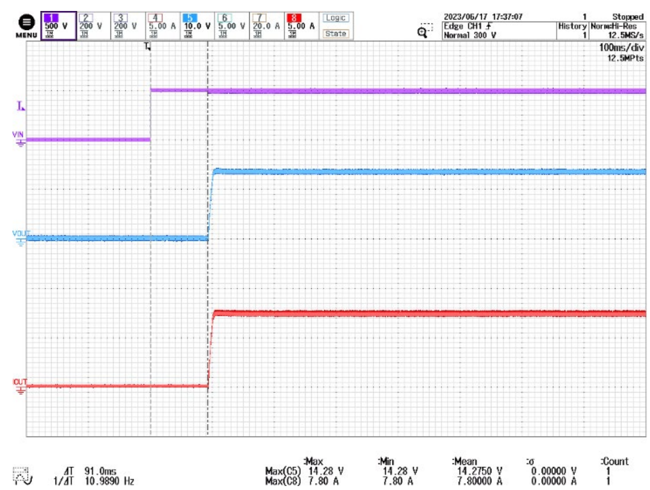


Figure 39 – Output Voltage and Current.
500 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH5: V_{OUT}, 10 V / div.
CH8: I_{OUT}, 5 A / div.
Time: 100 ms / div.

[15] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[16] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[17] Current waveforms were measured using a Yokogawa current probe

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient Temperature[18,19]

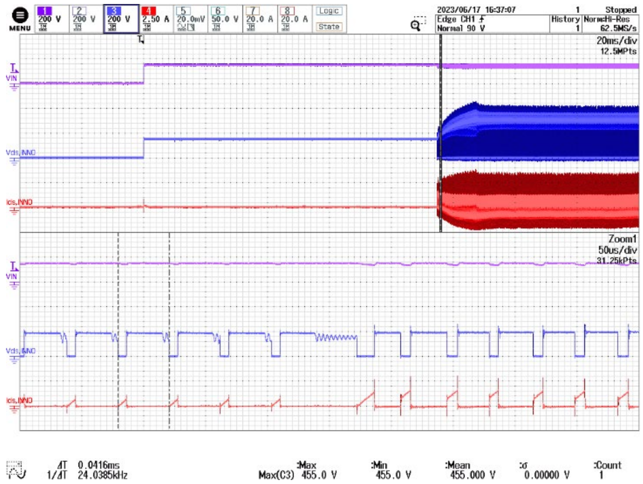


Figure 40 – INN3990CQ Drain Voltage and Current.
150 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 200 V / div.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 20 ms / div.

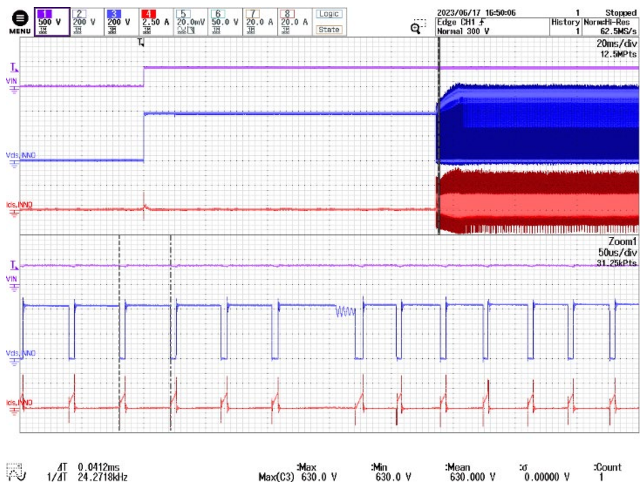


Figure 41 – INN3990CQ Drain Voltage and Current.
380 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 20 ms / div.

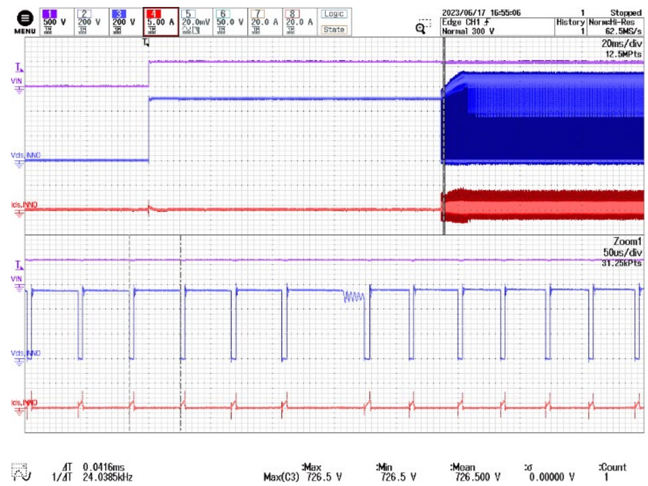


Figure 42 – INN3990CQ Drain Voltage and Current.
500 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 20 ms / div.

[18] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[19] Current waveforms were measured using a 30 A rogowski current probe.

11.1.3 SR FET Drain Voltage and Current at 85 °C Ambient Temperature[20,21]

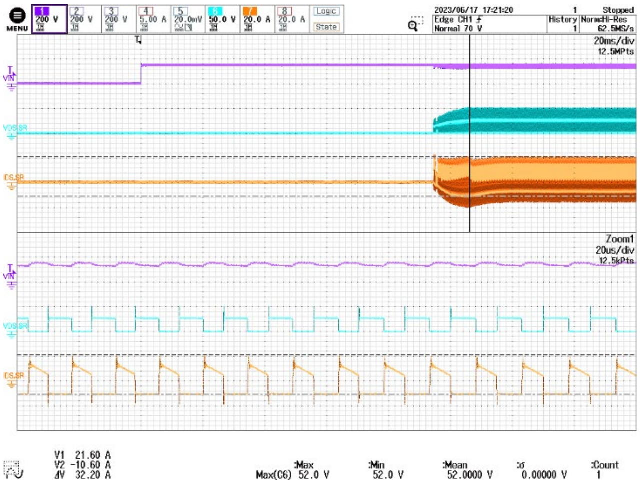


Figure 43 – SR FET Drain Voltage and Current.
Vin = 150 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 200 V / div.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

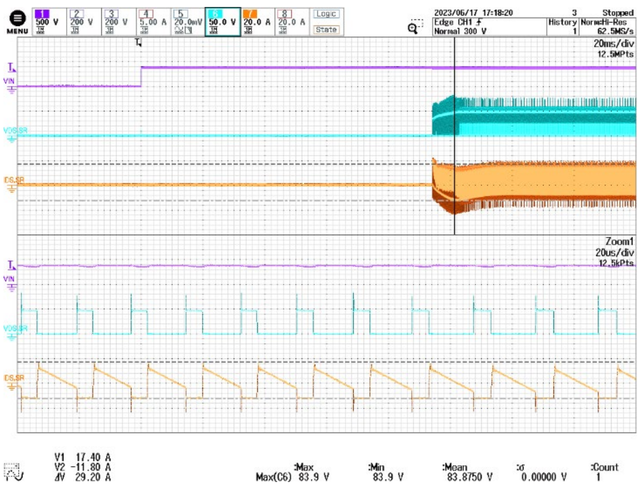


Figure 44 – SR FET Drain Voltage and Current.
Vin = 380 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

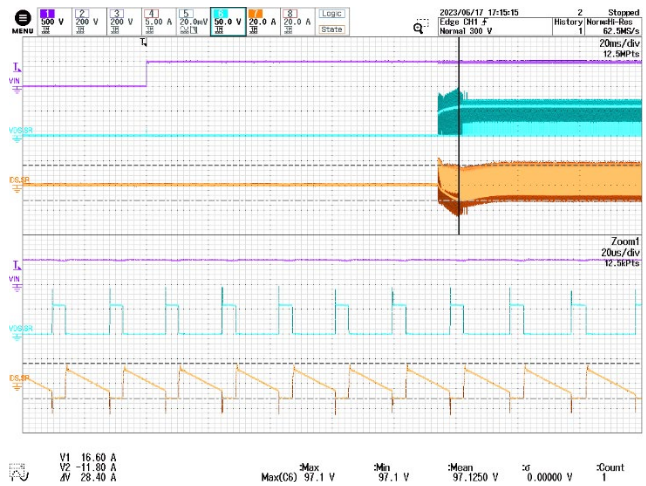


Figure 45 – SR FET Drain Voltage and Current.
Vin = 500 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

[20] The time between when V_{IN} is turned on and the SR FET starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[21] Current waveforms were measured using a 120 A rogowski current probe.

11.1.4 Output Voltage and Current at -40 °C Ambient Temperature[22,23]

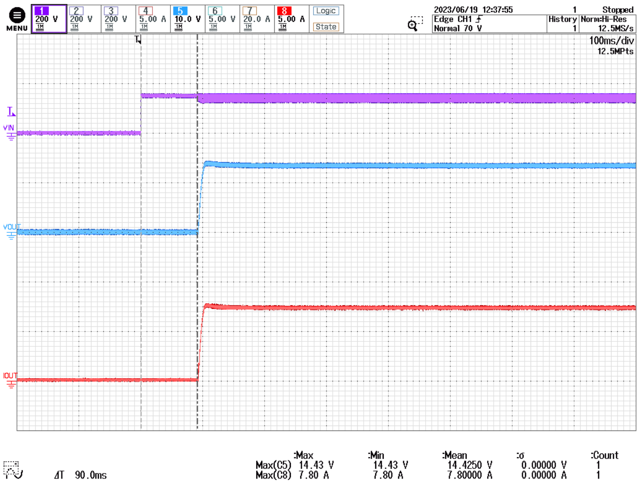


Figure 46 – Output Voltage and Current.
Vin = 150 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 200 V / div.
CH5: V_{OUT}, 10 V / div.
CH8: I_{OUT}, 5 A / div.
Time: 100 ms / div.

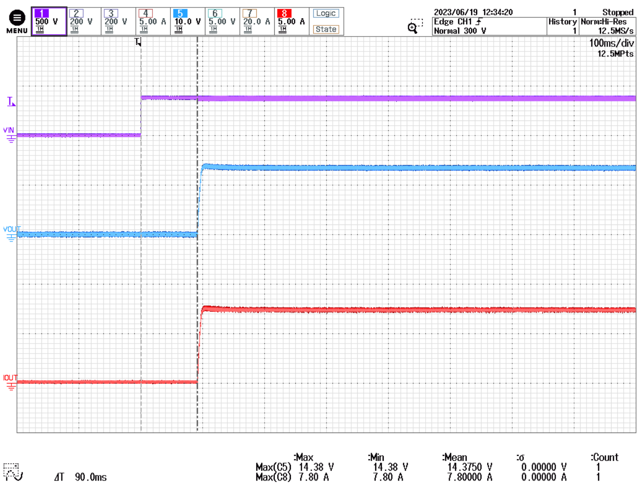


Figure 47 – Output Voltage and Current.
Vin = 380 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH5: V_{OUT}, 10 V / div.
CH8: I_{OUT}, 5 A / div.
Time: 100 ms / div.

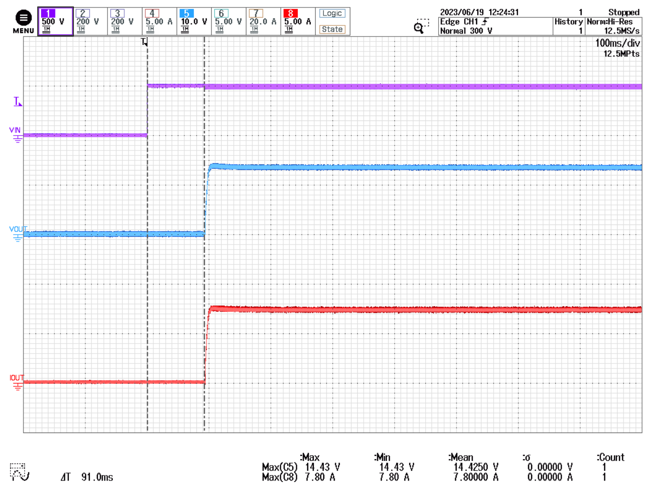


Figure 48 – Output Voltage and Current.
Vin = 500 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH5: V_{OUT}, 10 V / div.
CH8: I_{OUT}, 5 A / div.
Time: 100 ms / div.

[22] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[23] Current waveforms were measured using a Yokogawa current probe.

11.1.5 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient Temperature[24,25]

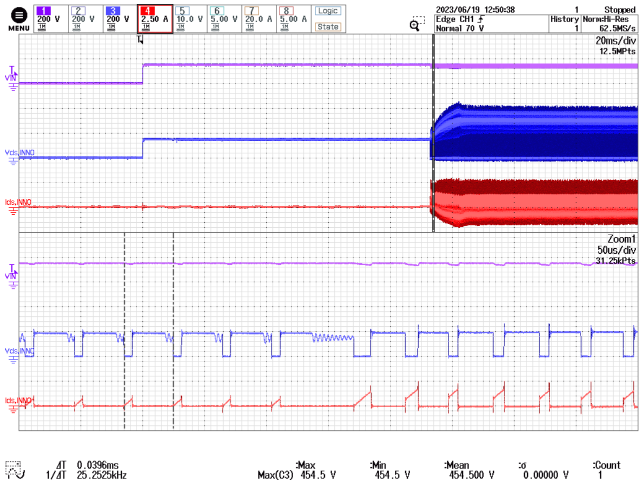


Figure 49 – INN3990CQ Drain Voltage and Current.
Vin = 150 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 200 V / div.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 20 ms / div.

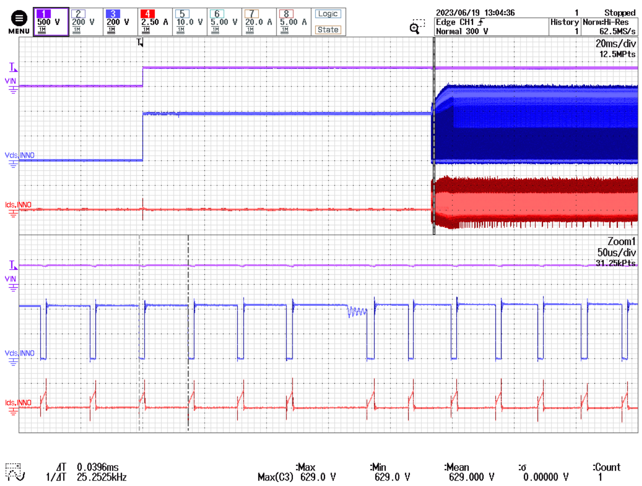


Figure 50 – INN3990CQ Drain Voltage and Current.
Vin = 380 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 20 ms / div.

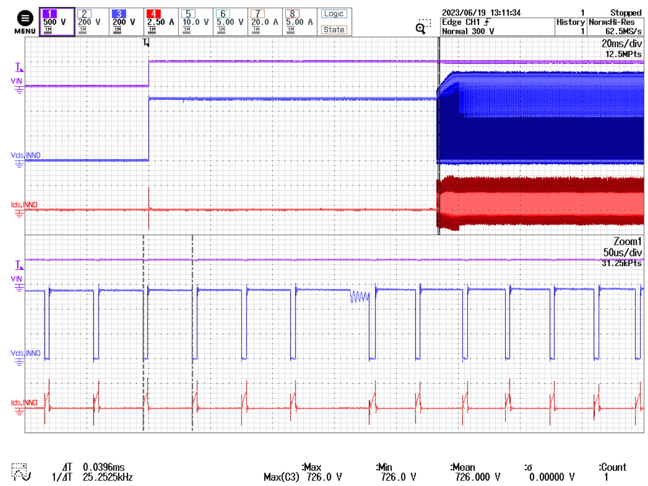


Figure 51 – INN3990CQ Drain Voltage and Current.
Vin = 500 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 20 ms / div.

[24] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[25] Current waveforms were measured using a 30 A Rogowski coil.

11.1.6 SR FET Drain Voltage and Current at -40 °C Ambient Temperature[26,27]

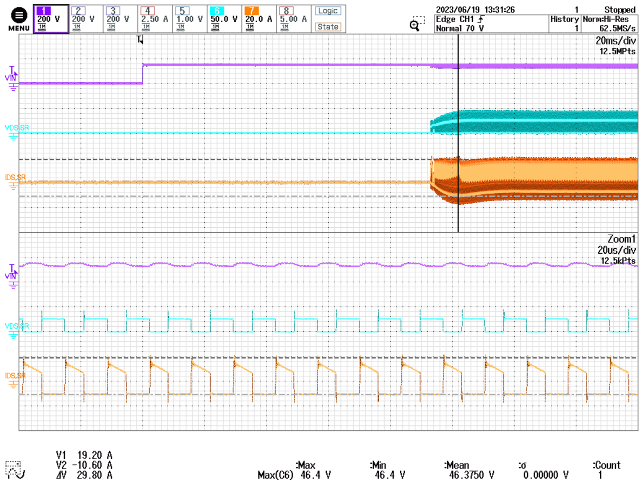


Figure 52 – SR FET Drain Voltage and Current.
Vin = 150 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 200 V / div.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

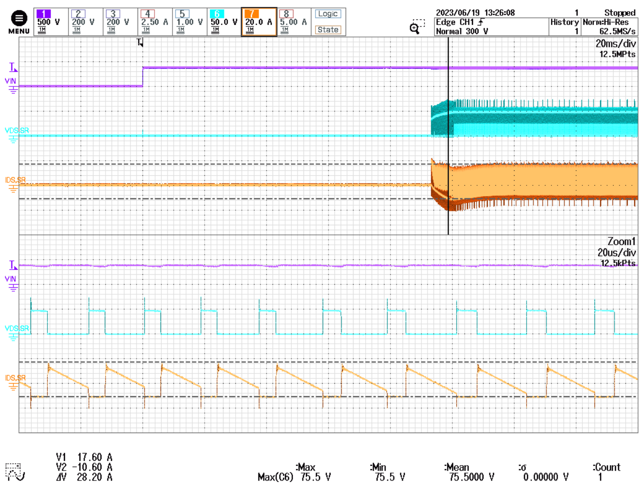


Figure 53 – SR FET Drain Voltage and Current.
Vin = 380 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

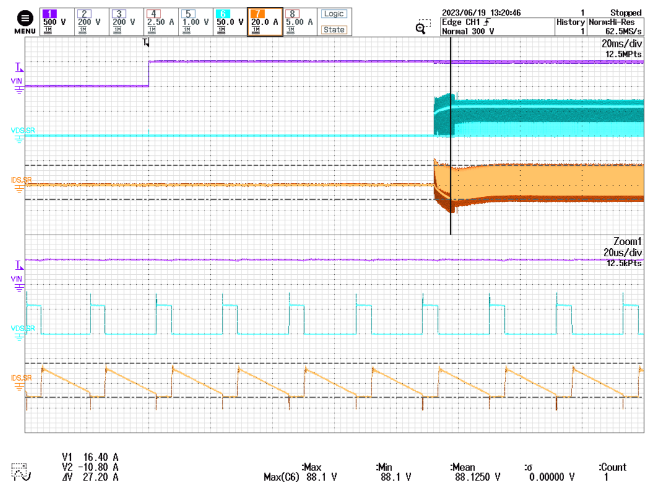


Figure 54 – SR FET Drain Voltage and Current.
Vin = 500 V_{DC}, 1.835 Ω Load.
CH1: V_{IN}, 500 V / div.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

[26] The time between when V_{IN} is turned on and the SR FET starts switching is due to the additiona t_{AR} delay of InnoSwitch3.
[27] Current waveforms were measured using a 120 A Rogowski coil.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 85 °C Ambient Temperature

11.2.1.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 85 °C Ambient, Full Load					
Input	**INN3990CQ**			**SR FETs**		
V_{IN}(V)	**I_D(A_{PK})**	**V_{DS}(V_{PK})**	**V_{STRESS} (%)**	**I_D(A_{PK})[28]**	**V_{DS}(V_{PK})[29]**	**V_{STRESS} (%)**
150	2.1	423	47	29	52	43.3
380	1.95	622	69.1	27.4	78	65
500	1.97	724	80.4	27.1	72.9	60.7

Table 11 – Summary of Critical Component Voltage Stresses at 85 °C Ambient Temperature.

[28] SR FET current is the sum of Q100 and Q101 currents.
[29] SR FET voltage was taken from Q101.

11.2.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient Temperature[30]

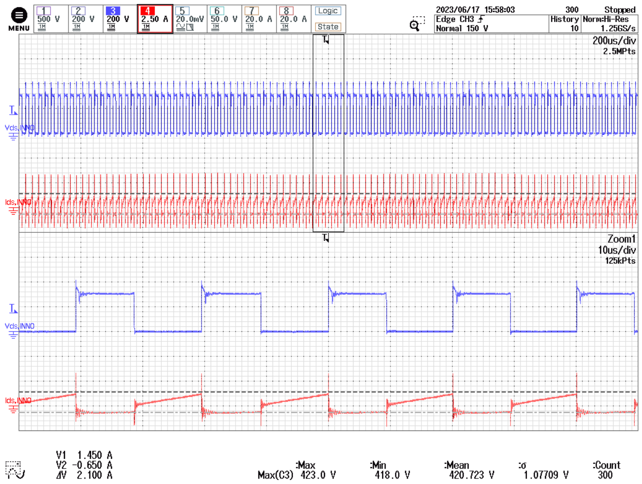


Figure 55 – INN3990CQ Drain Voltage and Current.
Vin = 150 V_{DC}, 7.35 A Load.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 200 μs / div.

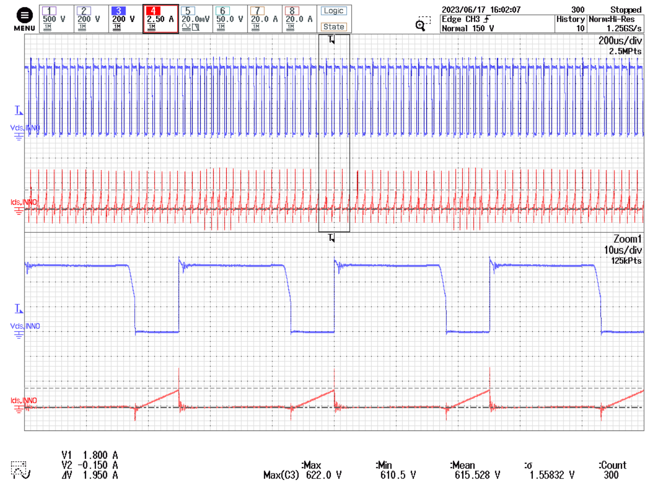


Figure 56 – INN3990CQ Drain Voltage and Current.
Vin = 380 V_{DC}, 7.35 A Load.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 200 μs / div.

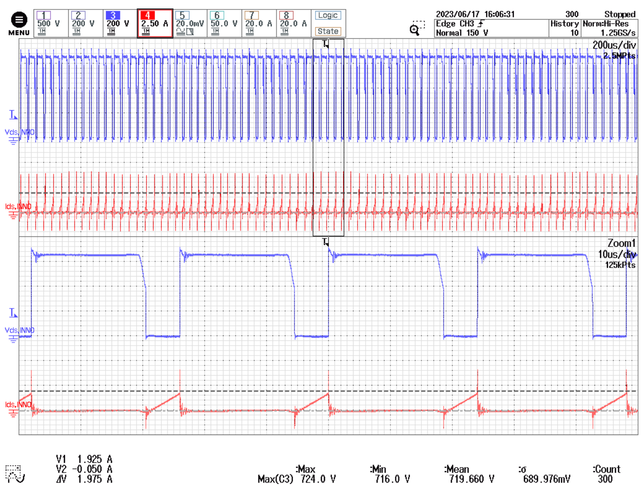


Figure 57 – INN3990CQ Drain Voltage and Current.
Vin = 500 V_{DC}, 7.35 A Load.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 200 μs / div.

30 Current is measured using a 30 A Rogowski probe

11.2.1.3 SR-FET Drain Voltage and Current at 85 °C Ambient Temperature[31]

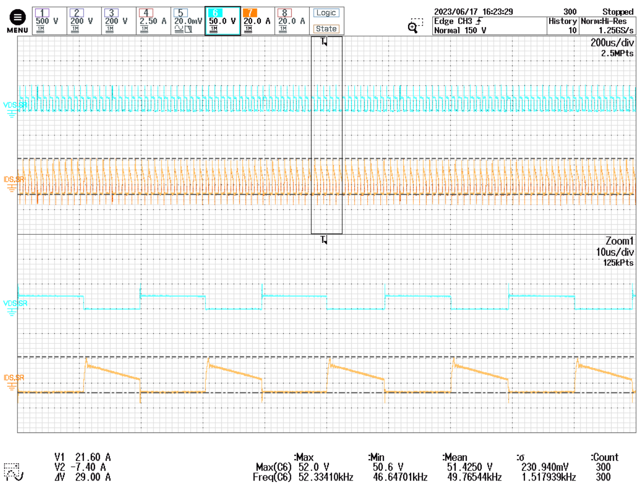


Figure 58 – SR FET Drain Voltage and Current.
Vin = 150 V_{DC}, 7.35 A Load.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 10 μs / div.

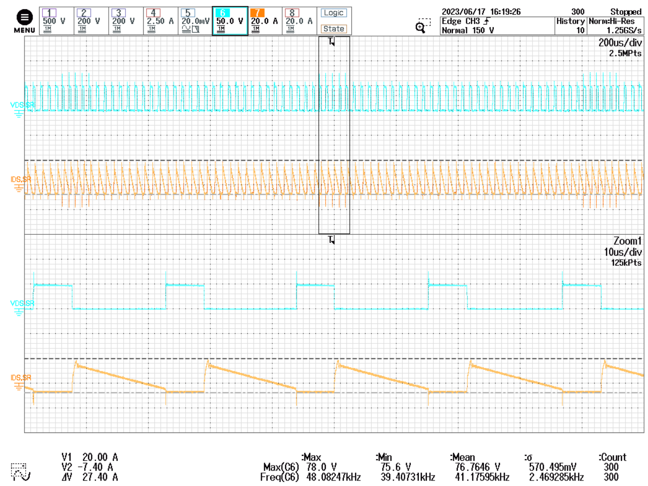


Figure 59 – SR FET Drain Voltage and Current.
Vin = 380 V_{DC}, 7.35 A Load.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 10 μs / div.

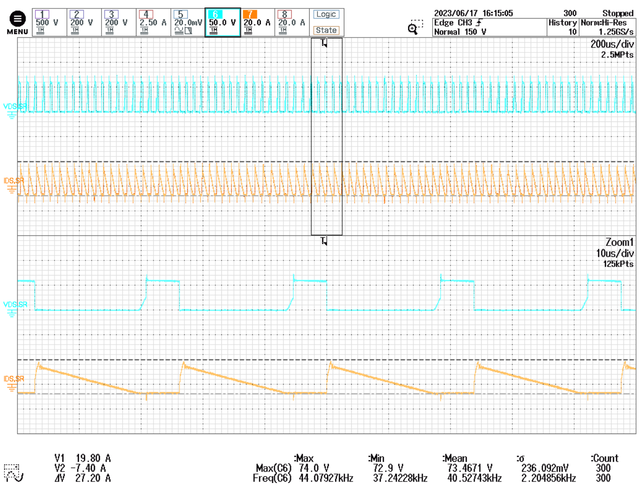


Figure 60 – SR FET Drain Voltage and Current.
Vin = 500 V_{DC}, 7.35 A Load.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 10 μs / div.

[31] Current is measured using a 120 A Rogowski probe

11.2.2 Switching Waveforms at -40 °C Ambient Temperature

11.2.2.1 Normal Operation Component Stress

	Steady-State Switching Waveforms -40 °C Ambient, Full Load					
Input	**INN3990CQ**			**SR FETs**		
V_{IN} (V)	**$I_D(A_{PK})$**	**$V_{DS}(V_{PK})$**	**V_{STRESS} (%)**	**$I_D(A_{PK})$[32]**	**$V_{DS}(V_{PK})$[33]**	**V_{STRESS} (%)**
150	2.17	427	47.4	28.4	46	38.3
380	2.07	624	69.3	25.2	74	61.6
500	2.07	726	80.6	25	73.5	61.2

Table 12 – Summary of Critical Component Voltage Stresses at -40 °C Ambient Temperature.

[32] SR FET current is the sum of Q100 and Q101 currents.
[33] SR FET voltage was taken from Q101.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient Temperature[34]

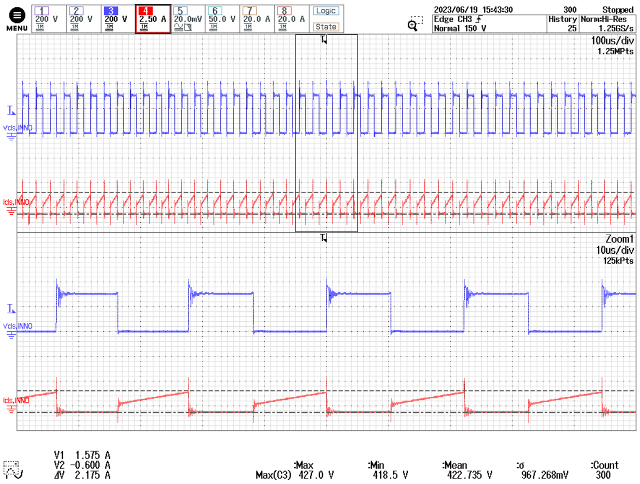


Figure 61 – INN3990CQ Drain Voltage and Current.
Vin = 150 V_{DC}, 7.35 A Load.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 100 µs / div.

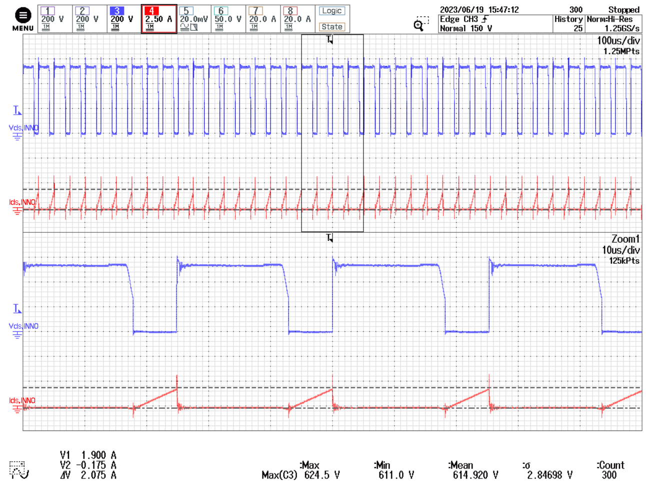


Figure 62 – INN3990CQ Drain Voltage and Current.
Vin = 380 V_{DC}, 7.35 A Load.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 100 µs / div.

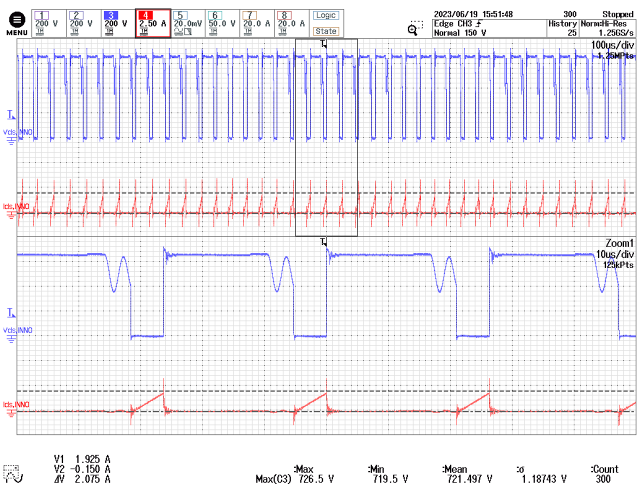


Figure 63 – INN3990CQ Drain Voltage and Current.
Vin = 500 V_{DC}, 7.35 A Load.
CH3: $V_{DS,INNO}$, 200 V / div.
CH4: $I_{DS,INNO}$, 2.5 A / div.
Time: 100 µs / div.

[34] Current is measured using a 30 A Rogowski probe

11.2.2.3 SR FET Drain Voltage and Current at -40 °C Ambient Temperature[35]

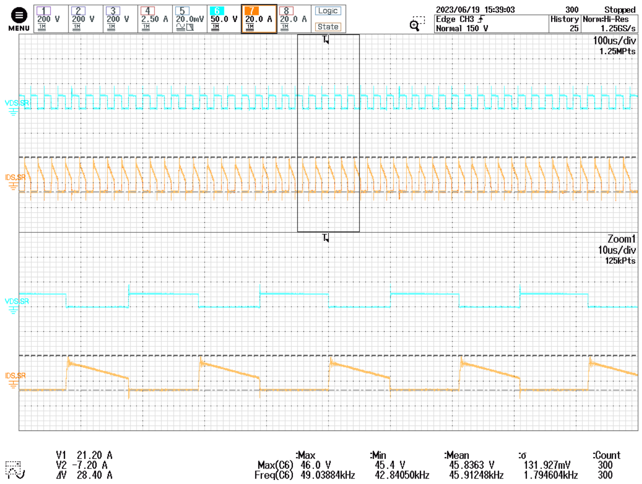


Figure 64 – SR FET Drain Voltage and Current.
Vin = 150 V_{DC}, 7.35 A Load.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

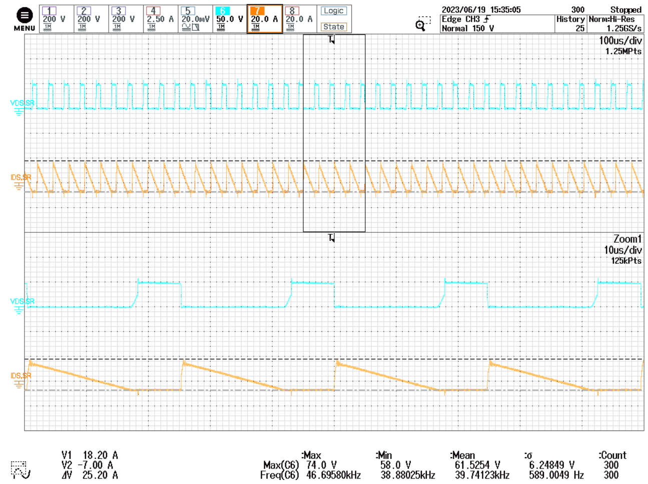


Figure 65 – SR FET Drain Voltage and Current.
Vin = 380 V_{DC}, 7.35 A Load.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

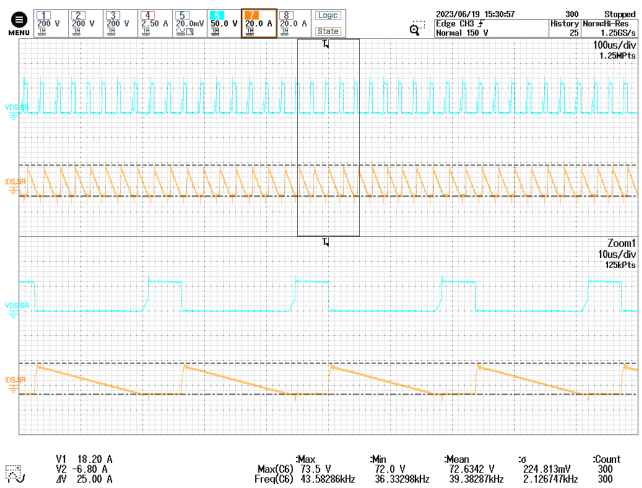


Figure 66 – SR FET Drain Voltage and Current.
Vin = 500 V_{DC}, 7.35 A Load.
CH6: $V_{DS,SR}$, 50 V / div.
CH7: $I_{DS,SR}$, 20 A / div.
Time: 20 ms / div.

[35] Current is measured using a 120 A Rogowski probe

11.2.2.4 Short-Circuit Response at 85 °C Ambient Temperature

The unit was tested by applying an output short-circuit during normal working conditions and then removing the short-circuit to see if the unit could recover and operate normally. The expected response during short-circuit is for the unit to go to AR (auto-restart) mode and attempt recovery every 1.7 to 2.11 seconds. Full load configuration is at 1.835 Ω constant resistance.

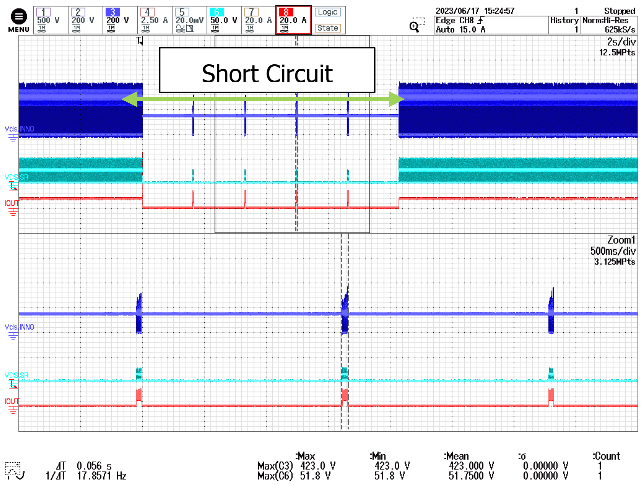


Figure 67 – INN3990CQ and SR FET Drain Voltage.
Vin = 150 V_{DC}, 1.835 Ω-Short-1.835 Ω.
CH3: $V_{DS,INNO}$, 200 V / div.
CH6: $V_{DS,SR}$, 50 V /div.
CH8: $I_{DS,SR}$, 20 A / div.
Time: 2 s / div.

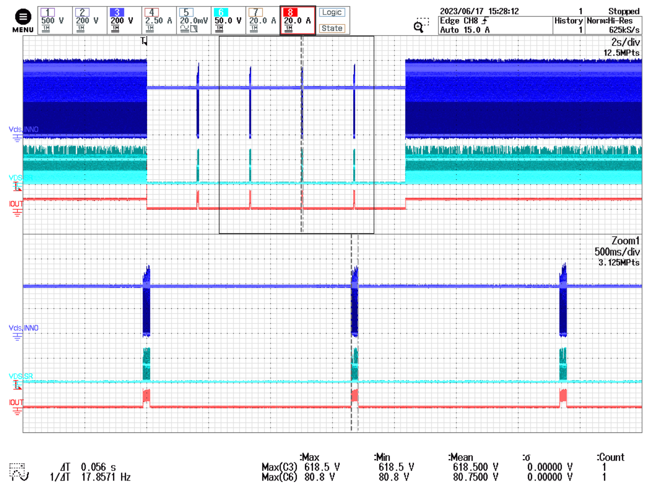


Figure 68 – INN3990CQ and SR FET Drain Voltage.
Vin = 380 V_{DC}, 1.835 Ω-Short-1.835 Ω .
CH3: $V_{DS,INNO}$, 200 V / div.
CH6: $V_{DS,SR}$, 50 V /div.
CH8: $I_{DS,SR}$, 20 A / div.
Time: 2 s / div.

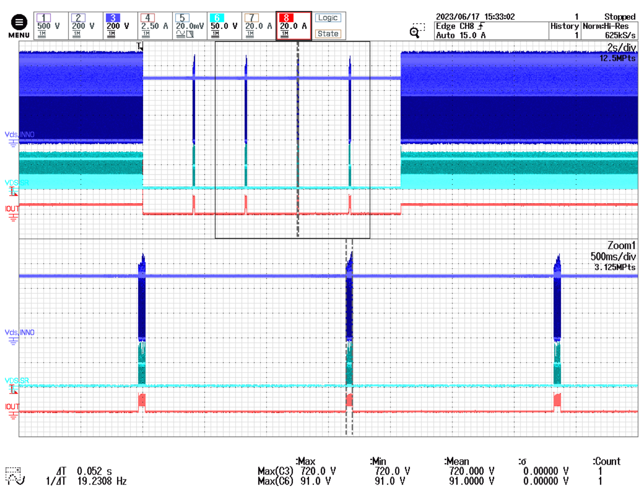


Figure 69 – INN3990CQ and SR FET Drain Voltage.
Vin = 500 V_{DC}, 1.835 Ω-Short-1.835 Ω.
CH3: $V_{DS,INNO}$, 200 V / div.
CH6: $V_{DS,SR}$, 50 V /div.
CH8: $I_{DS,SR}$, 20 A / div.
Time: 2 s / div.

11.3 Load Transient Response

Output voltage waveform on the board was captured with dynamic load transient from 0% to 90% and 10% to 90%. The duration for the load states is set to 500 ms, and the load slew rate is 400 mA / μs. The test is done at 85 °C ambient temperature with 10 samples taken per case.

Dynamic Load Settings	V_{IN} (V)	ΔV_{+} (V)	ΔV_{-} (V)
0% to 90%	150	0.246	-0.446
	190	0.255	-0.373
	380	0.255	-0.360
10% to 90%	150	0.225	-0.401
	190	0.243	-0.325
	380	0.239	-0.313

Table 13 – Load Transient Response.

11.3.1 Output Voltage Ripple with 0% to 90% Transient Load at 85 °C Ambient Temperature

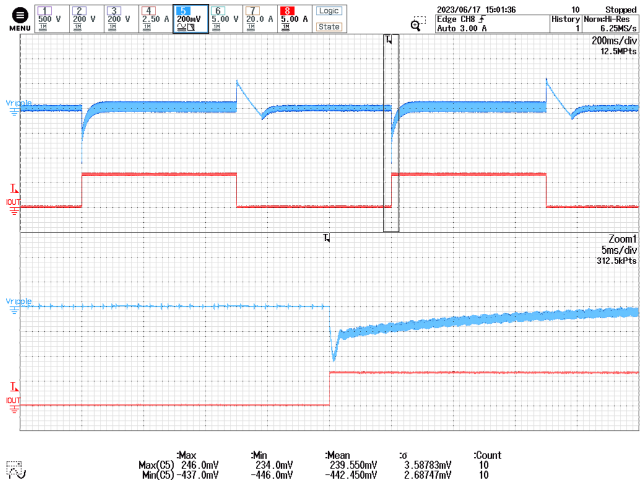


Figure 70 – Output Voltage and Current.
150 V_{DC}, 0 A to 7.35 A Transient Load,
85 °C Ambient.
CH5: V_{RIPPLE}, 200 mV / div.
CH8: I_{OUT}, 5 A / div.
Time: 200 ms / div.

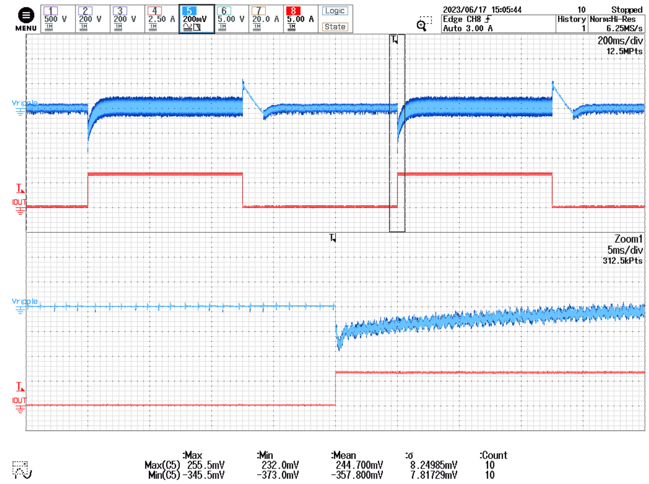


Figure 71 – Output Voltage and Current.
380 V_{DC}, 0 A to 7.35 A Transient Load,
85 °C Ambient.
CH1: V_{RIPPLE}, 200 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 200 ms / div.

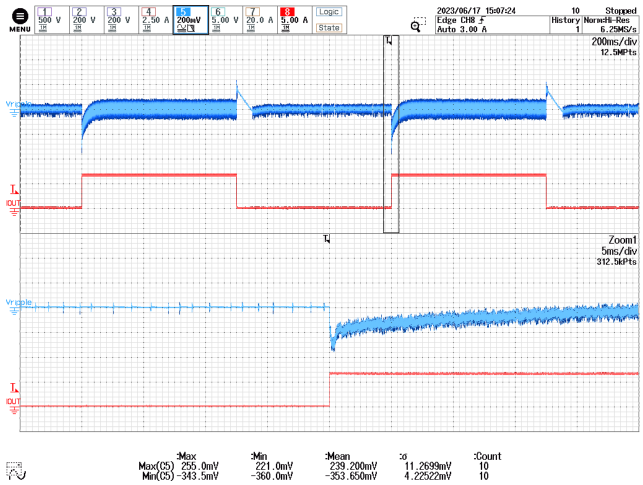


Figure 72 – Output Voltage and Current.
500 V_{DC}, 0 A to 7.35 A Transient Load,
85 °C Ambient.
CH1: V_{RIPPLE}, 200 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 200 ms / div.

11.3.2 Output Voltage Ripple with 10% to 90% Transient Load at 85 °C Ambient Temperature

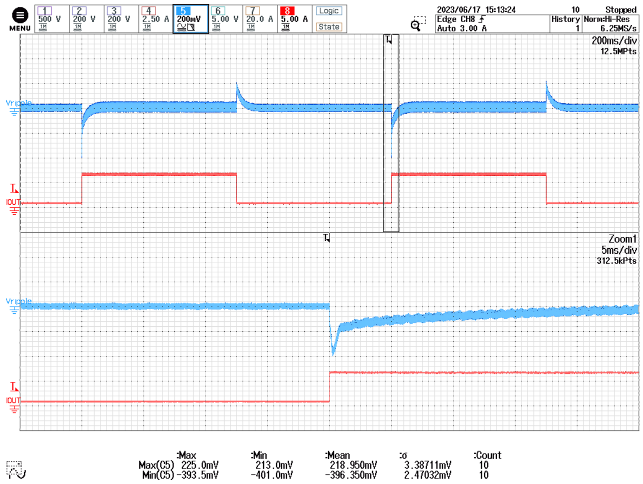


Figure 73 – Output Voltage and Current.
150 V_{DC}, 85 °C Ambient.
0.735 A to 7.35 A Transient Load
CH1: V_{RIPPLE}, 200 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 200 ms / div.

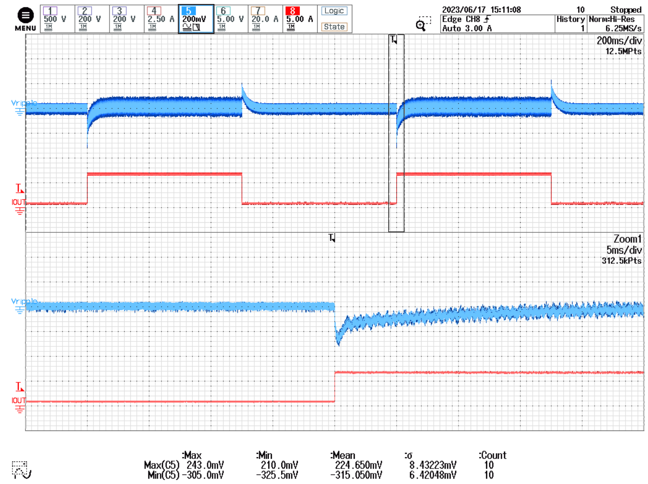


Figure 74 – Output Voltage and Current.
380 V_{DC}, 85 °C Ambient.
0.735 A to 7.35 A Transient Load
CH1: V_{RIPPLE}, 200 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 200 ms / div.

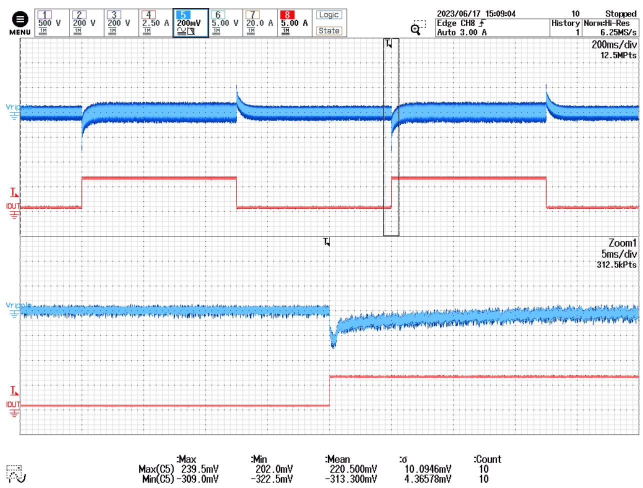


Figure 75 – Output Voltage and Current.
500 V_{DC}, 85 °C Ambient.
0.735 A to 7.35 A Transient Load
CH1: V_{RIPPLE}, 200 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 200 ms / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

A modified oscilloscope test probe must be utilized for DC output ripple measurements to reduce spurious signals due to noise pick-up. Details of the probe modification are provided in Figure 76 and Figure 77 below.

A CT2708 probe adapter is affixed with a 10 μF / 50 V electrolytic capacitor in parallel with a 1 μF / 50 V ceramic capacitor across the probe tip. Coaxial wires kept as short as possible are soldered directly to the probe and the output terminals.

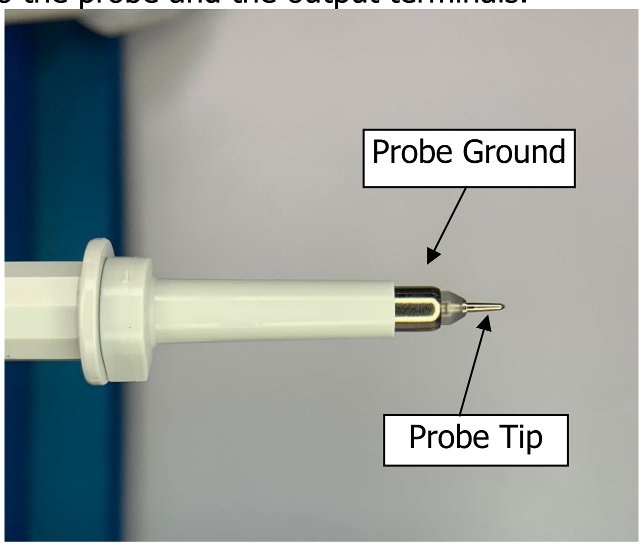


Figure 76 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

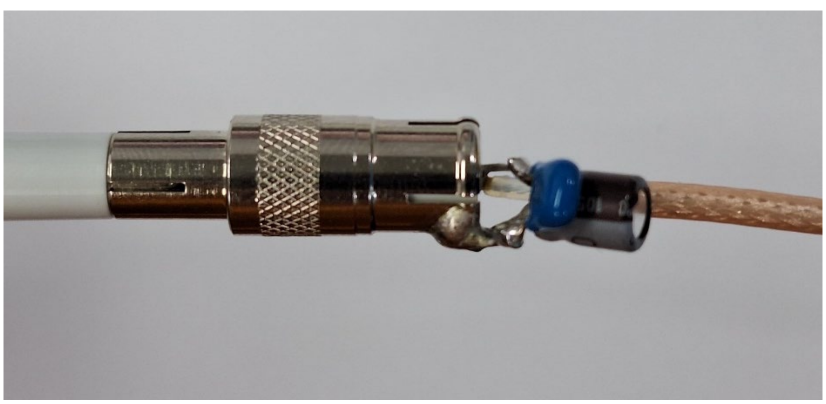


Figure 77 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurements, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform was captured at the output terminals using the ripple measurement probe with a decoupling capacitor. The waveforms shown are taken at the load setting where the highest ripple was observed for every input voltage setting.

11.4.2.1 Output Voltage Ripple at 85 °C Ambient Constant Full Load[36]

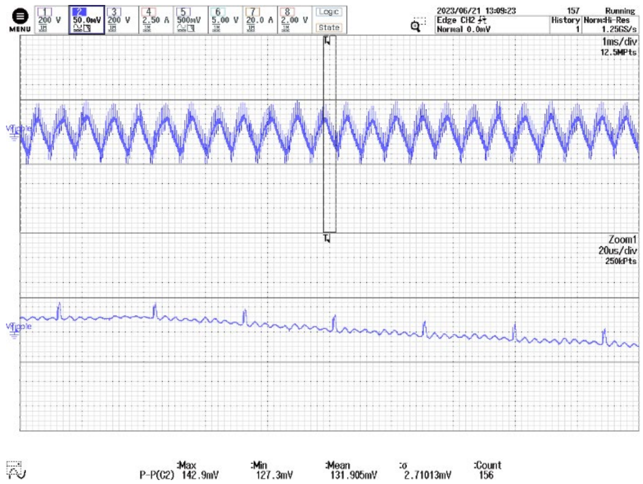


Figure 78 – Output Voltage Ripple.
150 V_{DC}, 5.15 A Load, 85 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 131 mV.

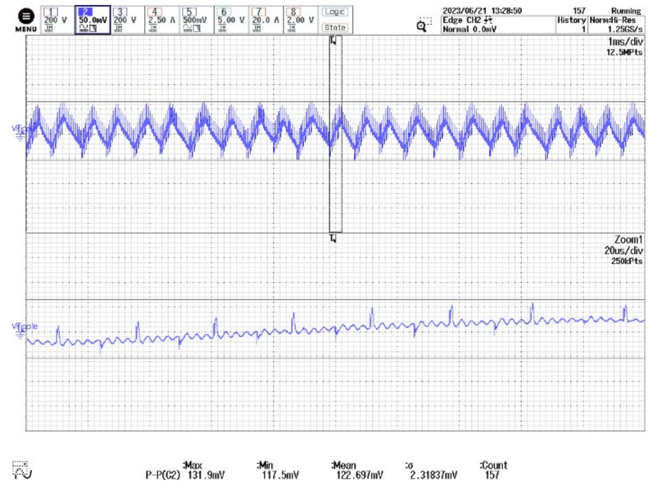


Figure 79 – Output Voltage Ripple.
190 V_{DC}, 5.88 A Load, 85 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 122 mV.

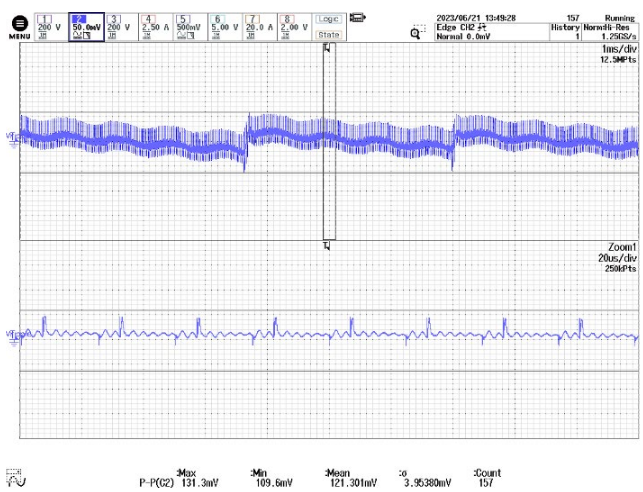


Figure 80 – Output Voltage Ripple.
380 V_{DC}, 7.35 A Load, 85 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 121 mV.

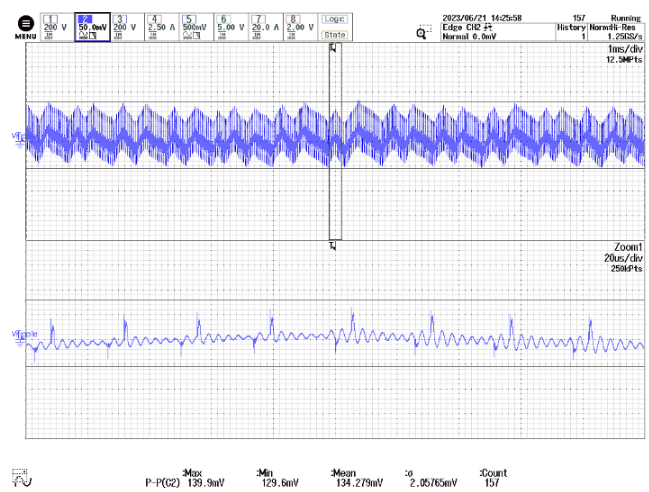


Figure 81 – Output Voltage Ripple.
500 V_{DC}, 7.35 A Load, 85 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 134 mV.

[36] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at -40 °C Ambient Constant Full Load[37]

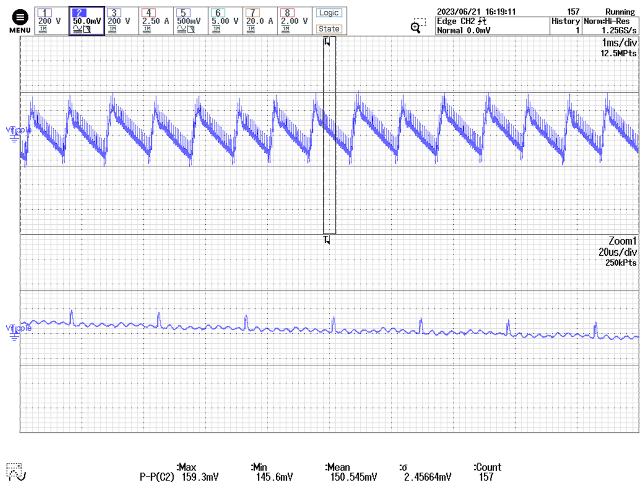


Figure 82 – Output Voltage Ripple.
150 V_{DC}, 4.41 A Load, -40 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 150 mV.

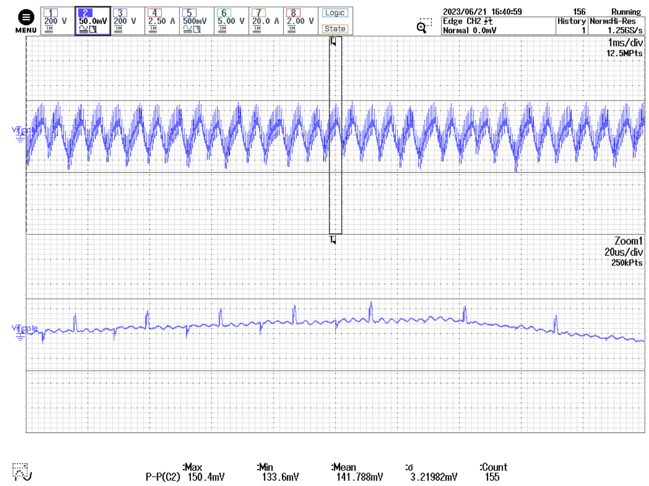


Figure 83 – Output Voltage Ripple.
190 V_{DC}, 6.61 A Load, -40 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 141 mV.

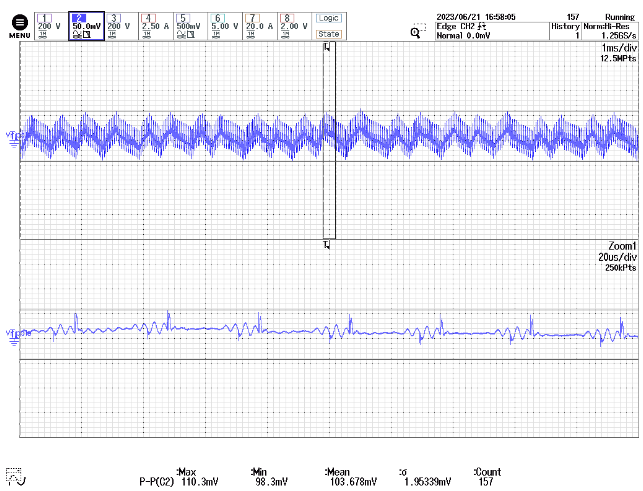


Figure 84 – Output Voltage Ripple.
380 V_{DC}, 5.88 A Load, -40 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 103 mV.

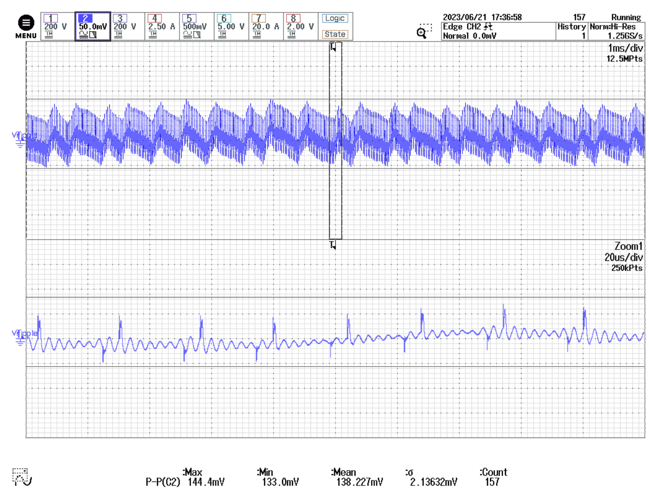


Figure 85 – Output Voltage Ripple.
500 V_{DC}, 7.35 A Load, -40 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 138 mV.

[37] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at 25 °C Ambient Constant Full Load[38]

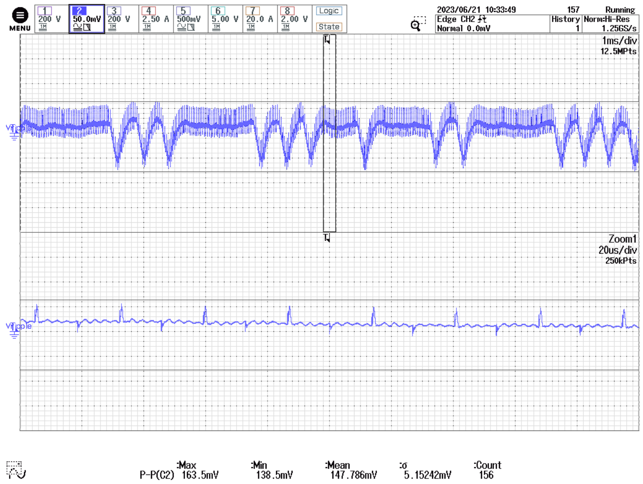


Figure 86 – Output Voltage Ripple.
150 V_{DC}, 5.88 A Load, 25 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 147 mV

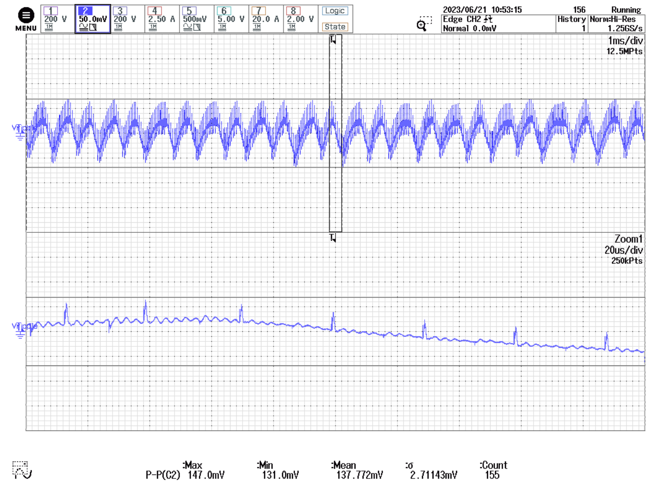


Figure 87 – Output Voltage Ripple.
190 V_{DC}, 6.61 A Load, 25 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 137 mV.

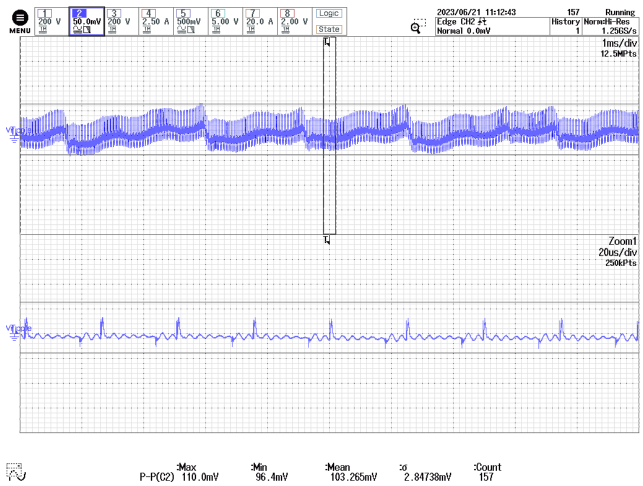


Figure 88 – Output Voltage Ripple.
380 V_{DC}, 7.35 A Load, 25 °C Ambient.
CH1: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 103 mV.

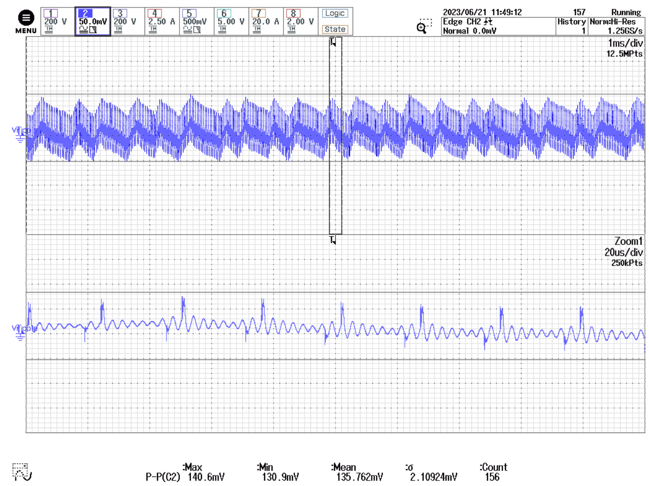


Figure 89 – Output Voltage Ripple.
500 V_{DC}, 7.35 A Load, 25 °C Ambient.
CH2: V_{RIPPLE}, 50 mV / div.
Time: 1 ms / div.
V_{RIPPLE} = 135 mV.

[38] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C Ambient

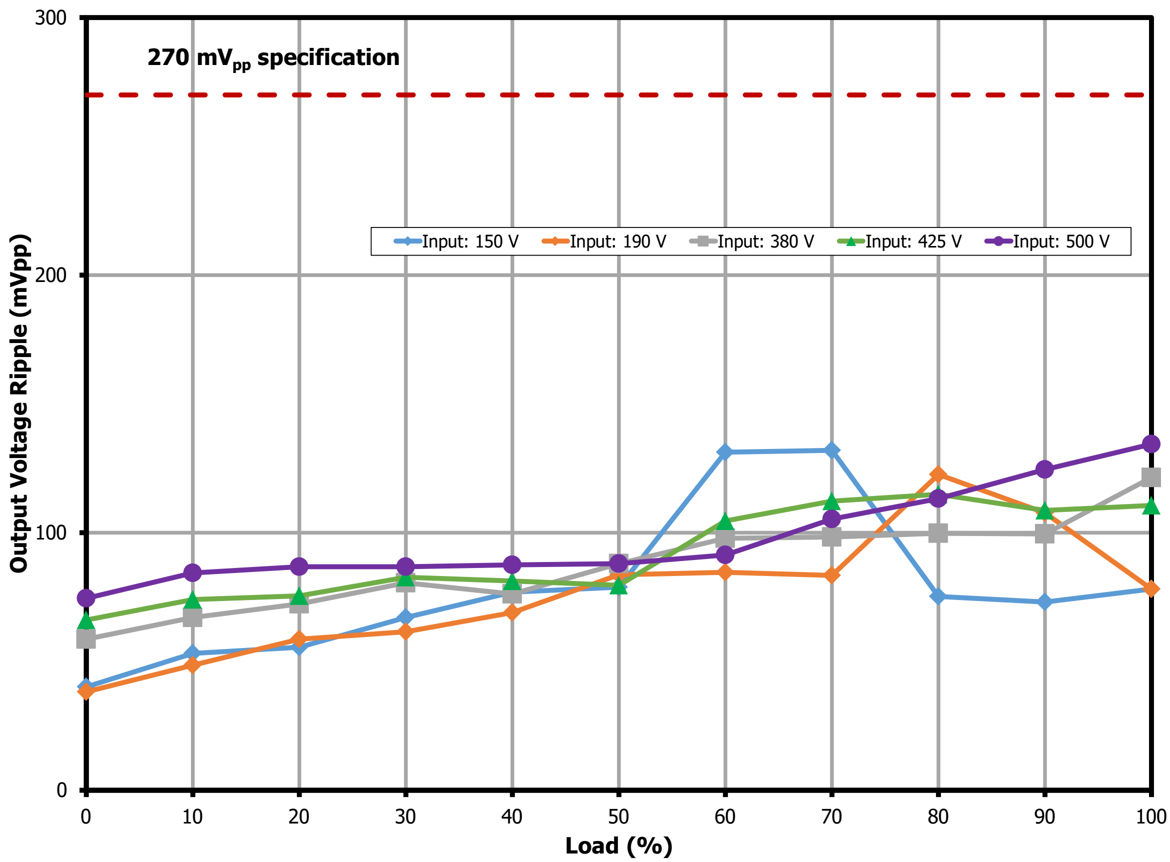


Figure 90 – Output Ripple Voltage Across Whole Load Range (85 °C Ambient).

11.4.3.2 Output Ripple at 25 °C Ambient

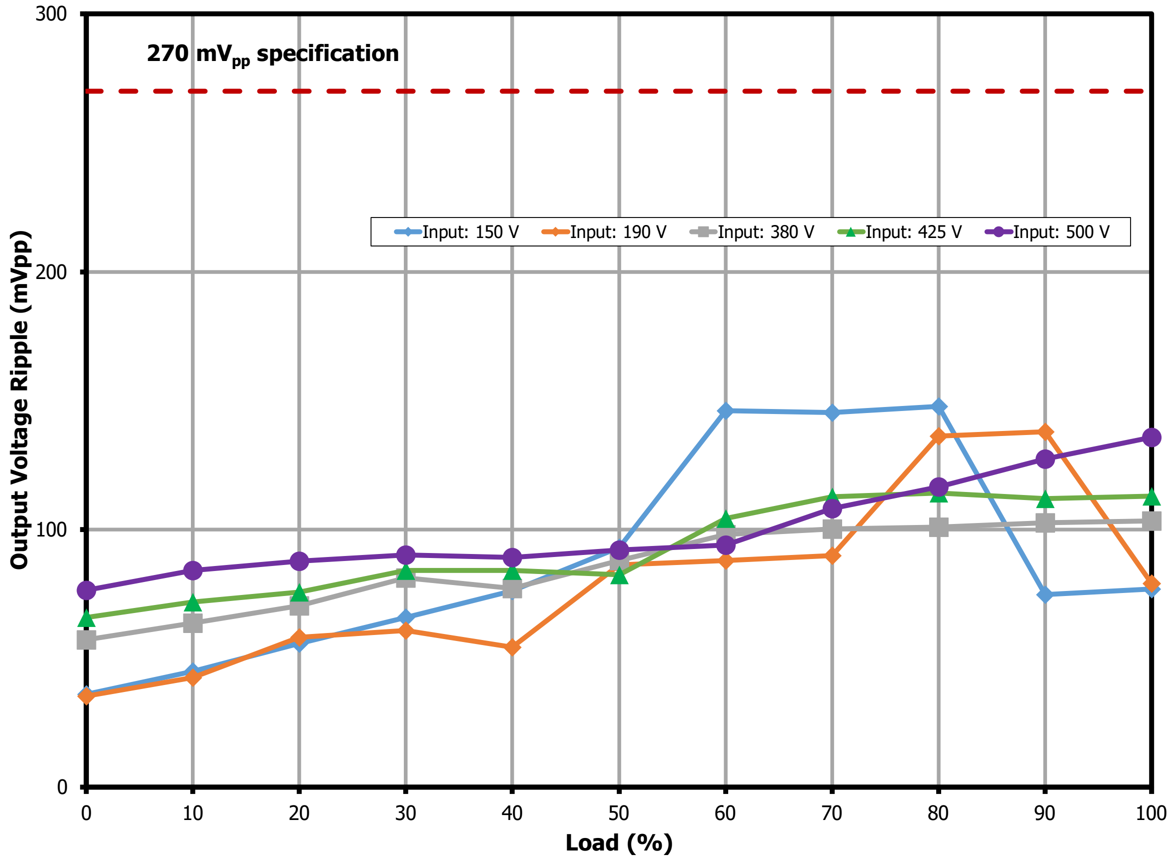


Figure 91 – Output Ripple Voltage Across Whole Load Range (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C Ambient

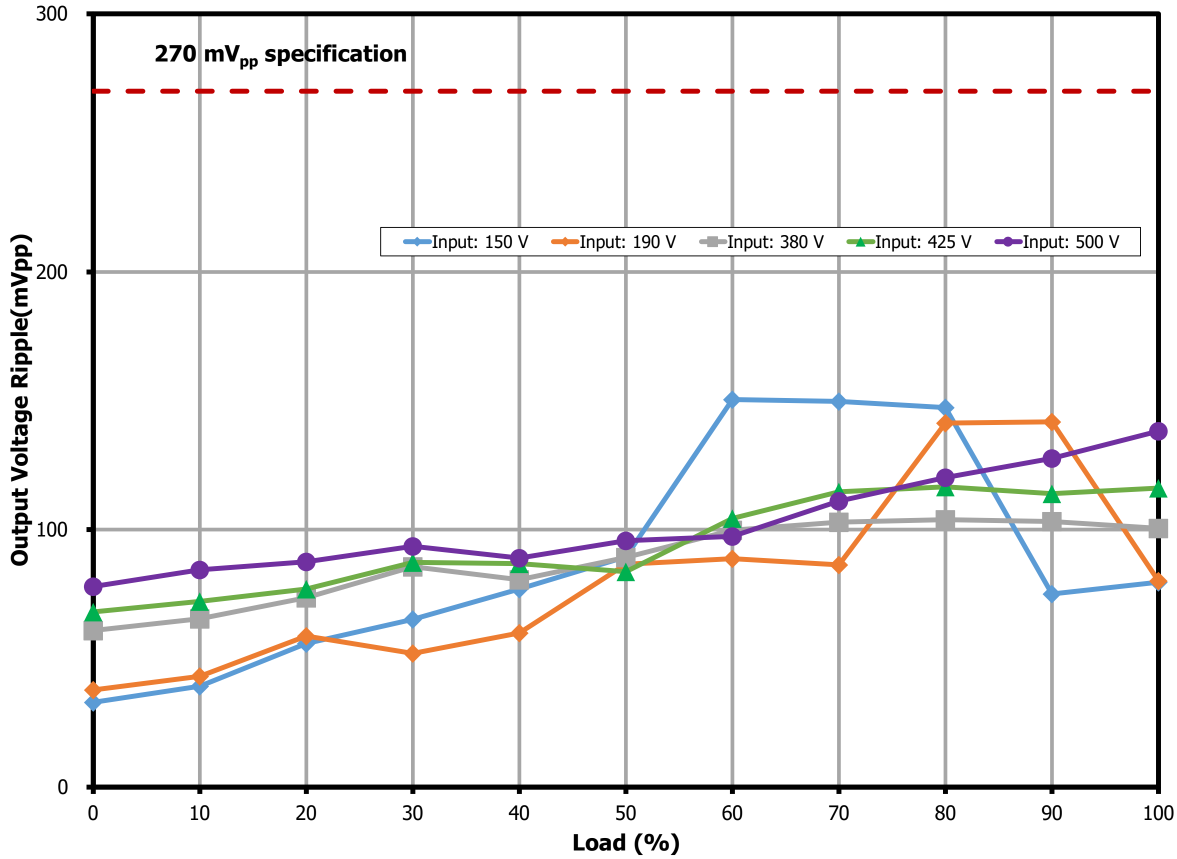


Figure 92 – Output Ripple Voltage Across Whole Load Range (-40 °C Ambient).

12 Maximum Output Power

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C for at least 30 minutes before turning on the unit under test. The unit was soaked for at least 30 minutes for every change in the input voltage and loading condition during the start of each test sequence to allow component temperatures to settle.

Maximum output power capability at a given input voltage was determined by finding the maximum loading condition in which the unit doesn't enter auto-restart (AR) mode operation or trigger any overtemperature protection. Component case temperature ratings for the critical components were also considered in determining the maximum output power capability.

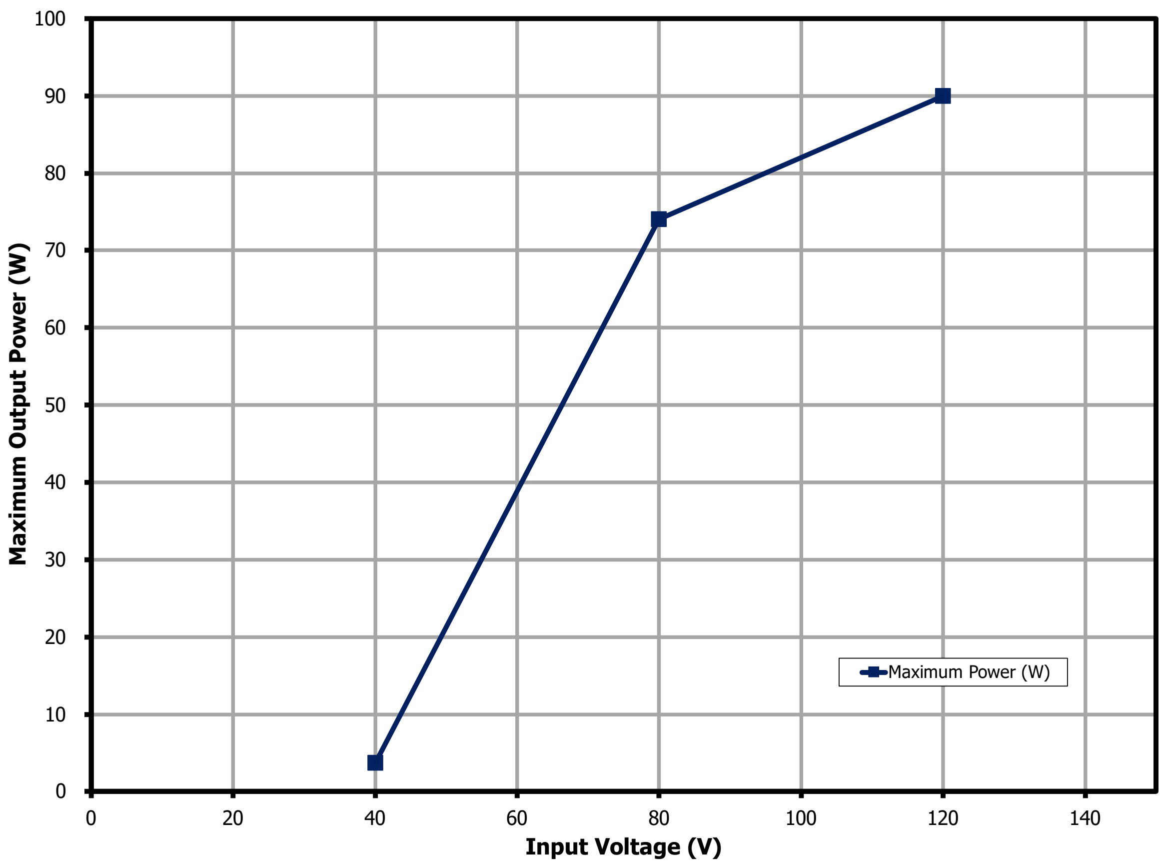


Figure 93 – Maximum Output Power Curve at 85 °C Ambient Temperature.

Input Voltage (V)	Maximum Power (W)	Limiting Factor	Value (ºC)
120	90	Transformer Winding Temperature	135.15
80	74	Transformer Winding Temperature	135.15
40	3.75	InnoSwitch3-AQ Power Limit	

Table 14 – Maximum Output Power Capability Limiting Factor.

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
14-Aug-23	MR	1.0	Initial Release.	CC/JRLC/MCR

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