

Summary of the Idea

The synchronous output rectifier (S2) of a power converter may be used to facilitate zero voltage switching (ZVS) of the main power switch (S1) of the power converter to reduce switching losses. The duration of time which the synchronous output rectifier S2 is turned ON to facilitate ZVS, e.g. T_{ZVS_ON} , along with the delay time between turning OFF the synchronous output rectifier S2 and turning ON the power switch S1, e.g. T_{ZVS_DLY} , may be programmable.

Description

Switching losses may result from having a non-zero voltage (V_{DS}) across the power switch S1 at the moment which the power switch S1 is turned ON due to the associated parasitic capacitance C_P of the power switch S1. A primary active clamp has been previously used to discharge the parasitic capacitance C_P to reduce the voltage (V_{DS}) across the power switch S1 to zero.

In lieu of a primary-side coupled active clamp, the secondary-side synchronous output rectifier S2 may be used to discharge the parasitic capacitance C_P to achieve ZVS. The duration of time which the synchronous output rectifier S2 is turned ON to facilitate ZVS, e.g. the ZVS on-time T_{ZVS_ON} , and the duration of time between turning OFF the synchronous output rectifier S2 and turning ON the power switch S1, e.g. ZVS delay time T_{ZVS_DLY} , are programmable. Programming may be accomplished using the Inter-Integrated Circuit (I2C) communication protocol.

Figure 1 illustrates a power converter with a secondary controller which controls the turn ON and turn OFF of the synchronous output rectifier S2 and allows programming of the ZVS on-time T_{ZVS_ON} and ZVS delay time T_{ZVS_DLY} . Figure 2 illustrates example waveforms of the voltage V_{DS} across power switch S1, request signal REQ, secondary drive signal SR, and primary drive signal DR.

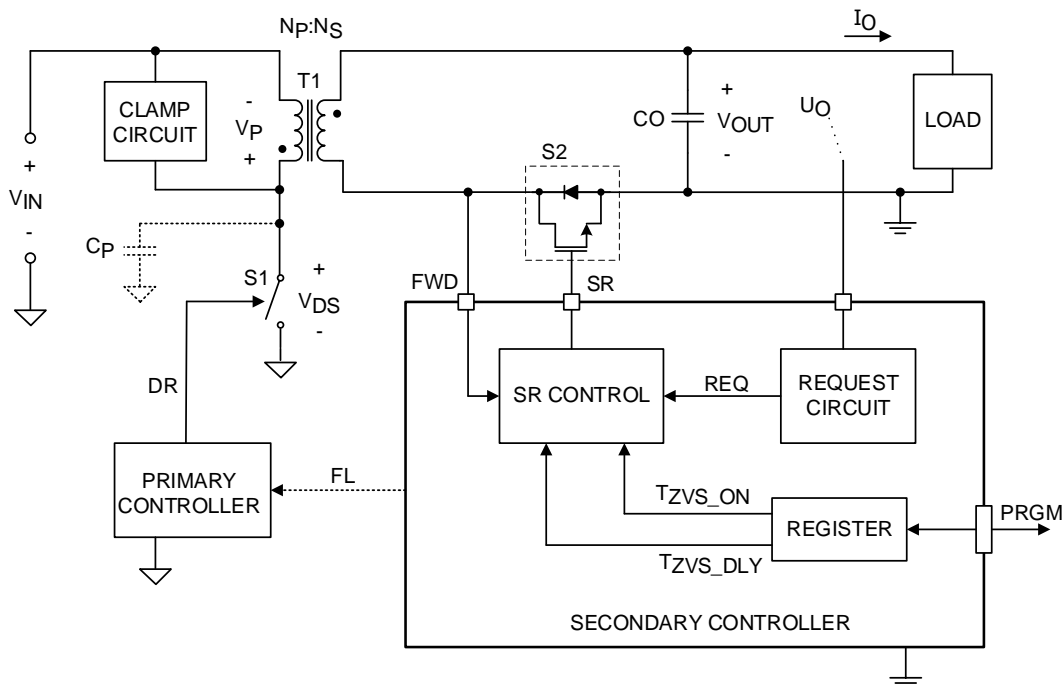


Figure 1. Programmable zero voltage switching (ZVS) using the synchronous output rectifier S2, the ZVS on-time T_{ZVS_ON} and the ZVS delay time T_{ZVS_DLY} may be programmed through a program terminal PRGM.

At time t_4 of Figure 2, the request circuit asserts the request signal REQ to turn ON the power switch S1 if the output voltage V_O falls below a regulation reference for the output of the power converter. If the power converter is also in discontinuous conduction mode (DCM), the synchronous output rectifier S2 is turned ON for the duration of the ZVS on-time T_{ZVS_ON} prior to the turn ON of the power switch S1 as shown by the high secondary drive signal SR. Between time t_4 and time t_5 , the magnetizing inductance of the transformer T1 is charged in the negative direction at a rate determined by the reflected output voltage on the primary of transformer T1. During this time, the drain voltage V_{DS} is substantially the sum of the input voltage V_{IN} and the voltage on the primary winding V_P .

Once the ZVS on-time T_{ZVS_ON} has elapsed, the ZVS delay time T_{ZVS_DLY} begins, the parasitic capacitance C_p is discharged and the drain voltage V_{DS} decreases. The duration of the ZVS delay time T_{ZVS_DLY} is programmed such that the drain voltage V_{DS} reaches zero prior to the power switch S1 turning ON. Once

the ZVS delay time T_{ZVS_DLY} has elapsed, the power switch S1 is turned on at time t_6 . As shown in Figure 1, a communication signal FL is sent to the primary controller from the secondary controller to turn ON the power switch S1.

The durations required for the ZVS on-time T_{ZVS_ON} and ZVS delay time T_{ZVS_DLY} to facilitate zero voltage switching may vary with the input voltage V_{IN} , output voltage V_{OUT} and the load. Usually the ZVS on-time T_{ZVS_ON} and ZVS delay time T_{ZVS_DLY} are either fixed durations or only a few trim options to cover the operating range of the power converter. These limited options can limit the potential of ZVS operation across line and load conditions and affect the efficiency of the overall power converter.

With secondary-side ZVS utilizing the synchronous output rectifier S2, the ZVS on-time T_{ZVS_ON} and ZVS delay time T_{ZVS_DLY} may be programmed through the I2C communication protocol. Potentially increasing efficiency for given line and load conditions.

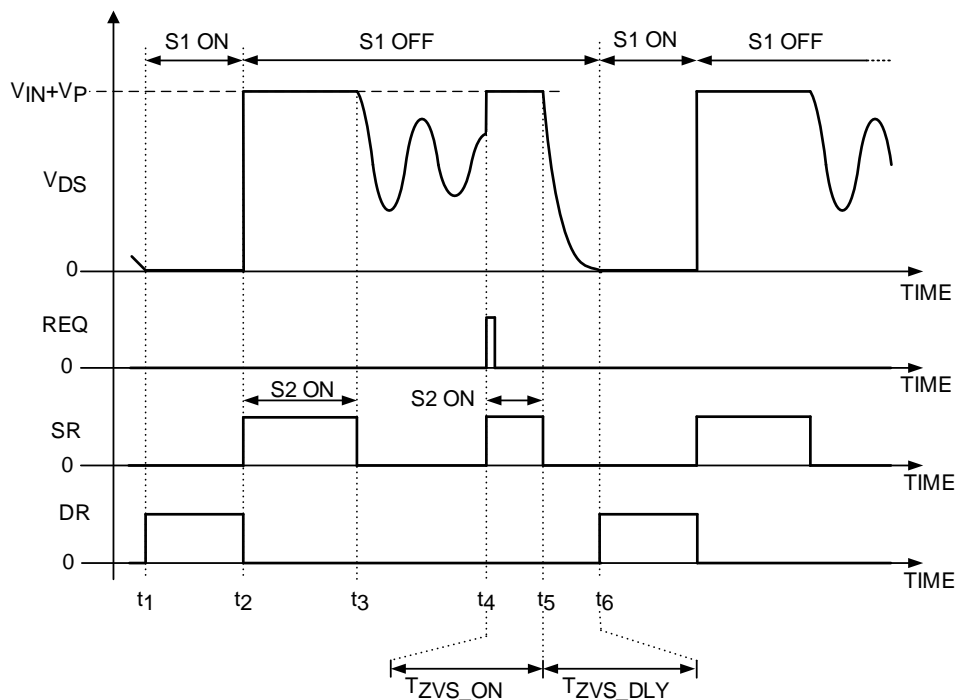


Figure 2. Timing diagram of various waveforms of Figure 1